Specification

conga-BM45

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Revision History

Revision	Date (dd.mm.yy)	Author	Changes
0.1	17.12.08	GDA	Preliminary release
0.2	29.01.09	GDA	Added section 8 “System Resources”
1.0	21.01.10	GDA	Official release. Added processor variant featuring Intel® Core™2 Duo Processor P8400. Updated information about the PCI Express Graphics (PEG) interface. Added pin numbers to sections 7, “Signal Descriptions and Pinout Tables.” Updated information throughout the user’s guide for the HDMI and DisplayPort interfaces. Updated section 8, “System Resources” and section 9 “BIOS Setup Description.”
1.1	22.06.10	GDA	Updated ISO certificate number. Added processor variant featuring Intel® Celeron Dual-Core T3100. Removed references to Microsoft® Windows® CE 5.0/6.0 from section 1.2 “Supported Operating Systems.” Microsoft® Windows® CE is not supported on the conga-BM45. Updated block diagram in section 2.

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Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-BM45. It is one of three documents that should be referred to when designing a COM Express™ application. The other reference documents that should be used include the following:

COM Express™ Design Guide
COM Express™ Specification

The links to these documents can be found on the congatec AG website at www.congatec.com

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Symbols

The following symbols are used in this user's guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

Terminology

Term	Description
GB	Gigabyte (1,073,741,824 bytes)
GHz	Gigahertz (one billion hertz)
kB	Kilobyte (1024 bytes)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
kHz	Kilohertz (one thousand hertz)
MHz	Megahertz (one million hertz)
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
PATA	Parallel ATA
T.O.M.	Top of memory = max. DRAM installed
HDA	High Definition Audio
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

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- AMIBIOS8_HDD_Security.pdf
- AMIBIOS8-Flash-Recovery-Whitepaper.pdf
- AMIBIOS8_SerialRedirection.pdf
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COM Express™ Concept

COM Express™ is an open industry standard defined specifically for COMs (computer on modules). It’s creation provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today. COM Express™ modules are available in following form factors:

- Compact 95mm x 95mm
- Basic 125mm x 95mm
- Extended 155mm x 110mm

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The COM Express™ specification 1.0 defines five different pinout types.

Types	Connector Rows	PCI Express Lanes	PCI	IDE Channels	LAN ports
Type 1	A-B	Up to 6			1
Type 2	A-B C-D	Up to 22	32 bit	1	1
Type 3	A-B C-D	Up to 22	32 bit		3
Type 4	A-B C-D	Up to 32		1	1
Type 5	A-B C-D	Up to 32			3

congatec AG modules utilize the Type 2 pinout definition. They are equipped with two high performance connectors that ensure stable data throughput.

The COM (computer on module) integrates all the core components and is mounted onto an application specific carrier board. COM modules are a legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to, a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The Type 2 pinout provides the ability to offer 32-bit PCI, Parallel ATA, and LPC options thereby expanding the range of potential peripherals. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, COM Express™ modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

Certification

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Lead-Free Designs (RoHS)

All congatec AG designs are created from lead-free components and are completely RoHS compliant.

Electrostatic Sensitive Device

All congatec AG products are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a congatec AG product except at an electrostatic-free workstation. Additionally, do not ship or store congatec AG products near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging. Be aware that failure to comply with these guidelines will void the congatec AG Limited Warranty.

conga-BM45 Options Information

The conga-BM45 is currently available in four different variants. This user's guide describes all of these options. Below you will find an order table showing the different configurations that are currently offered by congatec AG. Check the table for the Part no./Order no. that applies to your product. This will tell you what options described in this user's guide are available on your particular module.

Part-No.	013130	013140	013132	013135
Processor	Intel® Core™ 2 Duo T9400 2.53GHz (Socketed Micro-FCPGA478)	Intel® Core™ 2 Duo P8400 2.26GHz (Socketed Micro-FCPGA478)	Intel® Celeron 575 2.0GHz (Socketed Micro-FCPGA478)	Intel® Celeron Dual-Core T3100 1.9GHz (Socketed Micro-FCPGA478)
L2 Cache	6 MByte	3MB	1 MByte	1 MByte
FSB	1066MHz	1066MHz	667MHz	800MHz
DisplayPort (DP)	Yes	Yes	Yes	Yes
HDMI	Yes	Yes	Yes	Yes
Processor TDP	35 W	25 W	31 W	35 W

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1 Specifications

1.1 Feature List

Table 1 Feature Summary

Form Factor	Based on COM Express™ standard pinout Type 2 (Basic size 95 x 125mm)
Processor	Intel® Core™ 2 Duo T9400 2.53GHz with 6-MByte L2 cache (Socketed Micro-FCPGA478) Intel® Core™ 2 Duo P8400 2.26GHz with 3-MByte L2 cache (Socketed Micro-FCPGA478) Intel® Celeron Dual-Core T3100 1.9GHz with 1-MByte L2 cache (Socketed Micro-FCPGA478) Intel® Celeron 575 2.0GHz with 1-MByte L2 cache (Socketed Micro-FCPGA478)
Memory	2 sockets: SO-DIMM DDR3 1067MHz up to 8-GByte. Sockets located top and bottom side of module.
Chipset	Graphics and Memory Controller Hub (GMCH) Intel® GM45 Intel® I/O Controller Hub 82801IEM (ICH9M-E)
Audio	HDA (High Definition Audio)/digital audio interface with support for multiple codecs
Ethernet	Gigabit Ethernet: Integrated within the Intel® I/O Controller Hub 82801IEM (ICH9M-E) + Intel® 82567LM Phy. with AMT 4.0 support
Graphics Options	Mobile Intel® Graphics Media Accelerator 4500MHD, graphics core speeds up to 533 MHz, improved graphics and 3D rendering performance. Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0) OpenGL 2.0 and DirectX10 support. Two independent pipelines for full dual view support. • CRT Interface 300 MHz RAMDAC Resolutions up to 2048x1536 @ 70Hz (QXGA) • Flat panel Interface (integrated) 2x25-112MHz single/dual-channel LVDS Transmitter Single-channel LVDS interface support: 1 x 18 bpp OR 1 x 24 bpp (Type 1 only, compatible with VESA LVDS color mapping) Dual-channel LVDS interface support: 2 x 18 bpp OR 2 x 24 bpp panel support Supports both conventional (FPDI) and non-conventional (LDI) color mappings Automatic Panel Detection via EPI (Embedded Panel Interface based on VESA EDID™ 1.3) Resolutions 640x480 up to 1600x1200 (UXGA) • HDMI: Single TMDS Link, only support for RGB, video support for CEA modes 480i/p, 576i/p, 720p, 1080i/p and PC modes via dot clock and HDMI repeater support • Hardware acceleration for MPEG2 VLD/iDCT H/W motion compensation • DisplayPort (DP): Supports two DisplayPorts multiplexed with the PCI Express Graphics interface 1.62 Gb/s and 2.7 Gb/s, 1/2/4 data lanes, 8B10B-coding, Hot-Plug detect support, HDCP support • AUX Output 2 x Intel compliant SDVO ports (serial DVO) 200MPixel/sec each (shared with PEG x16 pins) Supports external DVI, TV and LVDS transmitter • TV Out: Integrated TV encoder supports HDTV (420p, 720p and 1080i), supports component and S-video
Peripheral Interfaces	• 3x Serial ATA® supports RAID 0/1/5/10 (4x Serial ATA® if SATA to PATA chip is not used) • 5x x1 PCI Express® Links (optionally, one additional x1, x2, x4, x8 link if x16 link is not used) • PCI Express Graphics x16 (shared with SDVO, DisplayPort, HDMI) • 8x USB 2.0 (EHCI) • PCI Bus Rev. 2.3 • 1x EIDE (UDMA-66/100) • LPC Bus • I²C Bus, Fast Mode (400 kHz) multimaster
BIOS	Based on AMIBIOS8® 1MByte Flash BIOS with congatec Embedded BIOS features
Power Management	ACPI 3.0 compliant with battery support. Also supports Suspend to RAM (S3).

Note

Some of the features mentioned in the above Feature Summary are optional. Check the article number of your module and compare it to the option information list on page 8 of this user's guide to determine what options are available on your particular module.

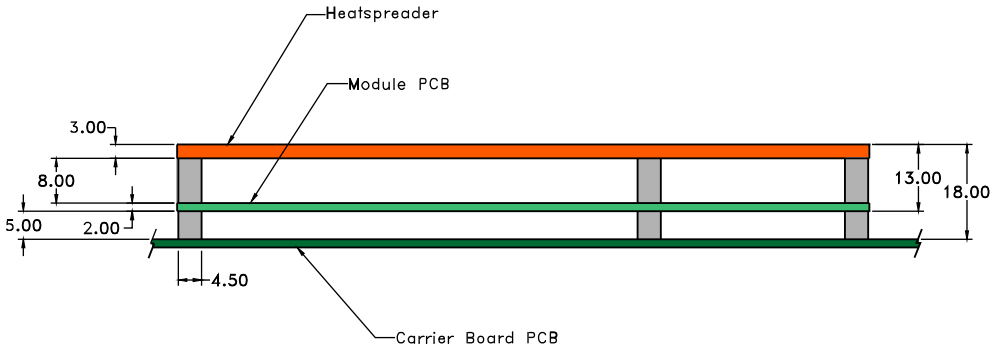
1.2 Supported Operating Systems

The conga-BM45 supports the following operating systems.

- Microsoft® Windows® Vista
- Microsoft® Windows® XP/2000
- Microsoft® Windows® XP Embedded
- Linux
- QNX

1.3 Mechanical Dimensions

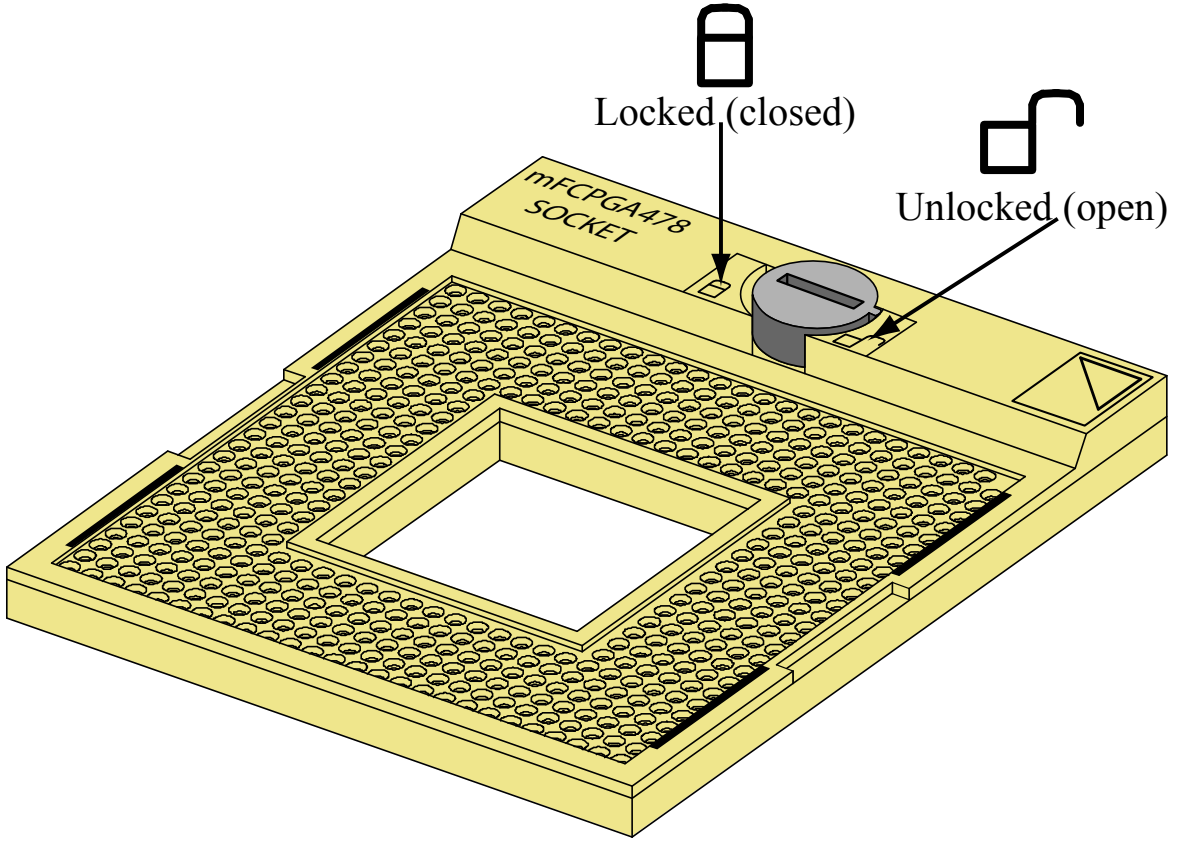
- 95.0 mm x 125.0 mm (3.74” x 4.92”)
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm.



1.4 Socketed Variant of conga-BM45

The conga-BM45 is equipped with a Micro-FCPGA socket. This socket has 478 contacts and mates with a Micro-FCPGA package that has a maximum of 478 pins. The insertion and extraction forces are zero when the socket is not engaged (in the “open” position).

There are clear indicator marks located on the actuation mechanism that identify the lock (closed) and unlock (open) positions of the cover as well as the actuation direction (see picture below). These marks remain visible after the processor is inserted into the socket.



Electrostatic Sensitive Device

The conga-BM45 is an electrostatic sensitive device. Do not handle the conga-BM45, or processor, except at an electrostatic-free workstation. Failure to do so may cause damage to the module and/or processor and void the manufacturer’s warranty.

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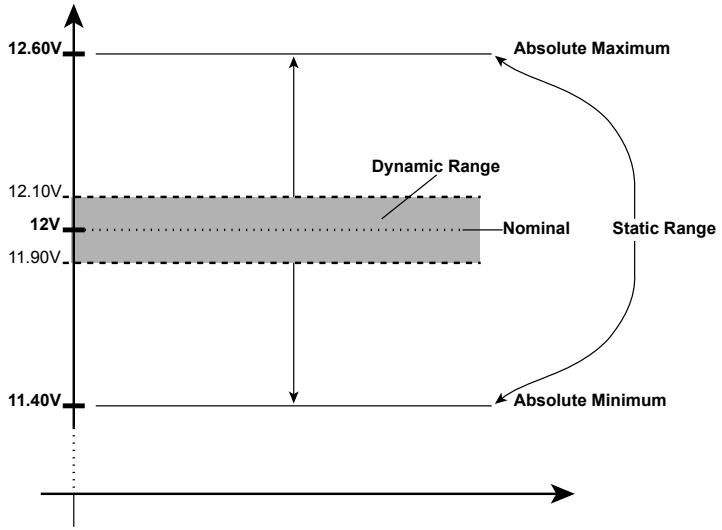
1.5 Supply Voltage Standard Power

- 12V DC ± 5%

The dynamic range shall not exceed the static range.



1.5.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 2 (dual connector, 440 pins).

Power Rail	Module Pin Current Capability (Amps)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	16.5	12	11.4-12.6	11.4	+/- 100	188	85%	160
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

1.5.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum rise time of 250V/s. The smooth turn-on requires that, during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

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1.6 Power Consumption

The power consumption values listed in this document were measured under a controlled environment. The hardware used includes a conga-BM45 module, conga-CEVAL and conga-Cdebug carrier boards, CRT monitor, SATA drive, and USB keyboard. When using the conga-Cdebug, the SATA drive was powered externally by an ATX power supply so that it does not influence the power consumption value that is measured for the module. The USB keyboard was detached once the module was configured within the OS. The module was first inserted into the conga-Cdebug, which was powered by a Direct Current (DC) power supply set to output 12V. The current consumption value displayed by the DC power supply's readout is the value that is recorded as the power consumption measurement for Desktop Idle, 100% Workload and Standby modes. The power consumption of the conga-Cdebug (without module attached) was measured and this value was later subtracted from the overall power consumption value measured when the module and all peripherals were connected. All recorded values are approximate.

The conga-Cdebug does not provide 5V Standby power therefore S3 mode was measured using the conga-CEVAL powered by an ATX power supply with a multimeter attached to the 5V Standby power line. The 5V Standby power consumption of the conga-CEVAL (without module attached) and all peripherals connected was first measured and the resulting value was later subtracted from the overall S3 power consumption value measured when the module was attached. All S3 recorded values are approximate.

Each module was measured while running Windows XP Professional with SP2 (service pack 2) and the "Power Scheme" was set to "Portable/ Laptop". This setting ensures that Core 2 Duo processor runs in LFM (lowest frequency mode) with minimal core voltage during desktop idle. Celeron processors do not support this feature and therefore always run at the same core voltage even during desktop idle. Each module was tested while using a Micron® DDR3 PC3-1066 1GB memory module. Using different sizes of RAM, as well as two memory modules, will cause slight variances in the measured results.

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Power consumption values were recorded during the following stages:

Windows XP Professional SP2

- Desktop Idle (1000MHz for 667MHz FSB or 800MHz for 533MHz FSB modules)
- 100% CPU workload (see note below)
- Windows XP Professional Standby Mode (requires setup node “Suspend Mode” in the BIOS to be configured to S1 POS (Power On Suspend))
- Suspend to RAM (requires setup node “Suspend Mode” in BIOS to be configured to S3 STR (suspend to RAM)). Supply power for S3 mode is 5V.

Note

A software tool was used to stress the CPU to 100% workload.

Processor Information

In the following power tables there is some additional information about the processors. Intel® offers processors that are considered to be low power consuming. These processors can be identified by their voltage status. Intel uses the following terms to describe these processors. If none of these terms are used then the processor is not considered to be low power consuming.

LV=Low voltage

ULV=Ultra low voltage

When applicable, the above mentioned terms will be added to the power tables to describe the processor. For example:

Intel® Core™ 2 Duo T9400 2.53GHz 6MB L2 cache

LV 45nm

Intel® also describes the type of manufacturing process used for each processor. The following term is used:

nm=nanometer

The manufacturing process description is included in the power tables as well. See example below. For information about the manufacturing process visit Intel®'s website.

Intel® Core™ 2 Duo T9400 2.53GHz 6MB L2 cache

LV **45nm**

1.6.1 Intel® Core™ 2 Duo T9400 2.53GHz 6MB L2 cache

With 1GB memory installed

conga-BM45 Art. No. 013130	Intel® Core™ 2 Duo T9400 2.53GHz 6MB L2 cache 45nm Layout Rev. BM45LX0 /BIOS Rev. BM45R004			
Memory Size	1GB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.8 A/9.6 W (12V)	3.5 A/42.7 W (12V)	1.1 A/13.2 W (12V)	0.2 A/1 W (5V)

1.6.2 Intel® Core™ 2 Duo P8400 2.26GHz 3MB L2 cache

With 1GB memory installed

conga-BM45 Art. No. 013140	Intel® Core™ 2 Duo P8400 2.26GHz 3MB L2 cache 45nm Layout Rev. BM45LX0 /BIOS Rev. BM45R004			
Memory Size	1GB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	0.9 A/10.8 W (12V)	3.0 A/36 W (12V)	0.9 A/10.8 W (12V)	0.2 A/1 W (5V)

1.6.3 Intel® Celeron® Dual-Core™ T3100 1.9GHz 1MB L2 cache

With 1GB memory installed

conga-BM45 Art. No. 013135	Intel® Dual-Core™ T3100 1.9GHz 1MB L2 cache 45nm Layout Rev. BM45LB0 /BIOS Rev. BM45R111			
Memory Size	1GB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	1.0 A/12.0 W (12V)	2.7 A/32.4 W (12V)	0.9 A/10.8 W (12V)	0.2 A/1 W (5V)

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1.6.4 Intel® Celeron® 575 2.0GHz 1MB L2 cache

With 512MB memory installed

conga-BM45 Art. No. 013132	Intel® Celeron 575 2.0GHz 1MB L2 cache 65nm Layout Rev. BM45LX0 /BIOS Rev. BM45R004			
Memory Size	1GB			
Operating System	Windows XP Professional SP2			
Power State	Desktop Idle	100% workload	Standby	Suspend to Ram (S3) 5V Input Power
Power consumption (measured in Amperes/Watts)	1.0 A/12 W (12V)	2.3 A/27.6 W (12V)	1.1 A/13.2 W (12V)	0.2 A/1 W (5V)

Note

All recorded power consumption values are approximate and only valid for the controlled environment described earlier. 100% workload refers to the CPU workload and not the maximum workload of the complete module. Supply power for S3 mode is 5V while all other measured modes are supplied with 12V power. Power consumption results will vary depending on the workload of other components such as graphics engine, memory, etc.

1.7 Supply Voltage Battery Power

- 2.0V-3.5V DC
- Typical 3V DC

1.7.1 CMOS Battery Power Consumption

RTC @ 20°C	Voltage	Current
Integrated in the Intel® I/O Controller Hub 82801IEM (ICH9M-E)	3V DC	2.8 µA

The CMOS battery power consumption value listed above should not be used to calculate CMOS battery lifetime. You should measure the CMOS battery power consumption in your customer specific application in worst case conditions, for example during high temperature and high battery voltage. The self-discharge of the battery must also be considered when determining CMOS battery lifetime. For more information about calculating CMOS battery lifetime refer to application note AN9_RTC_Battery_Lifetime.pdf, which can be found on the congatec AG website at www.congatec.com.

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1.8 Environmental Specifications

Temperature	Operation: 0° to 60°C	Storage: -20° to +80°C
Humidity	Operation: 10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a heatspreader the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

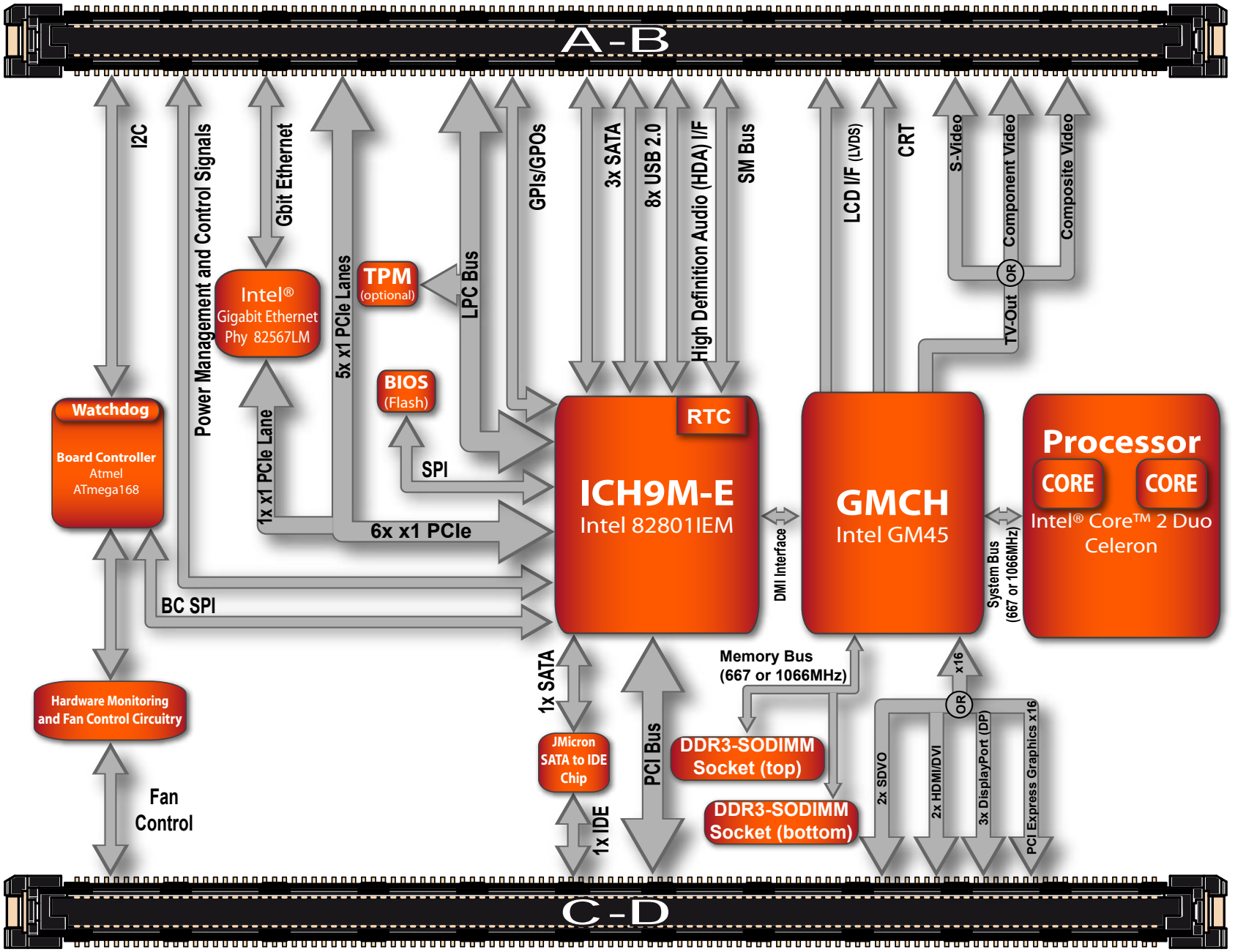
congatec AG strongly recommends that you use the appropriate congatec module heatspreader as a thermal interface between the module and your application specific cooling solution.

If for some reason it is not possible to use the appropriate congatec module heatspreader, then it is the responsibility of the operator to ensure that all components found on the module operate within the component manufacturer's specified temperature range.

For more information about operating a congatec module without heatspreader contact congatec technical support.

Humidity specifications are for non-condensing conditions.

2 Block Diagram



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3 Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the module. It is a 3mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

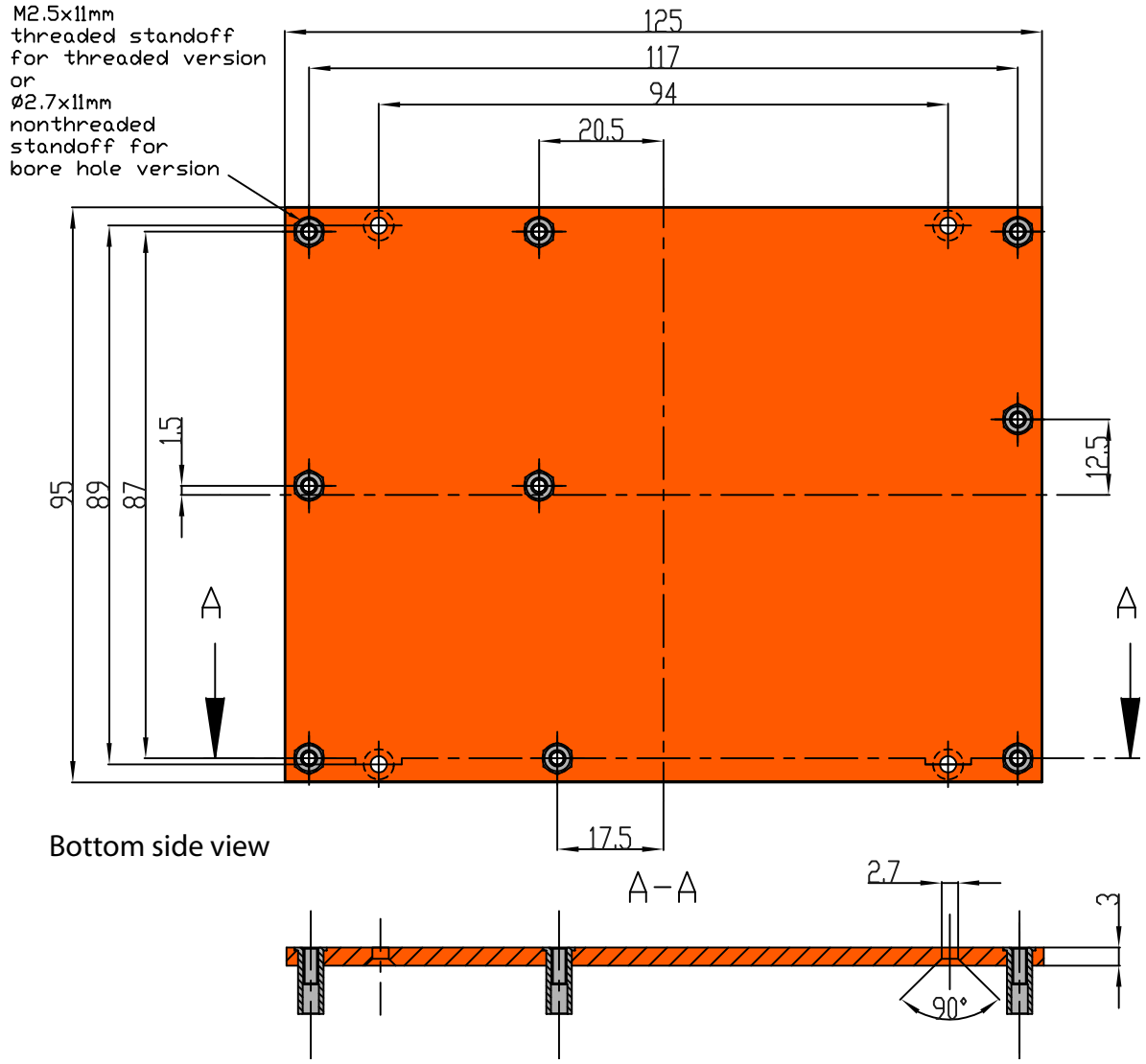
Although the heatspreader is the thermal interface where most of the heat generated by the module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

Caution

There are 4 mounting holes on the heatspreader designed to attach the heatspreader to the module. These mounting holes must be used to ensure that all components that are required to make contact with heatspreader do so. Failure to utilize the these mounting holes will result in improper contact between these components and heatspreader thereby reducing heat dissipation efficiency.

Attention must be given to the mounting solution used to mount the heatspreader and module into the system chassis. Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

3.1 Heatspreader Dimensions

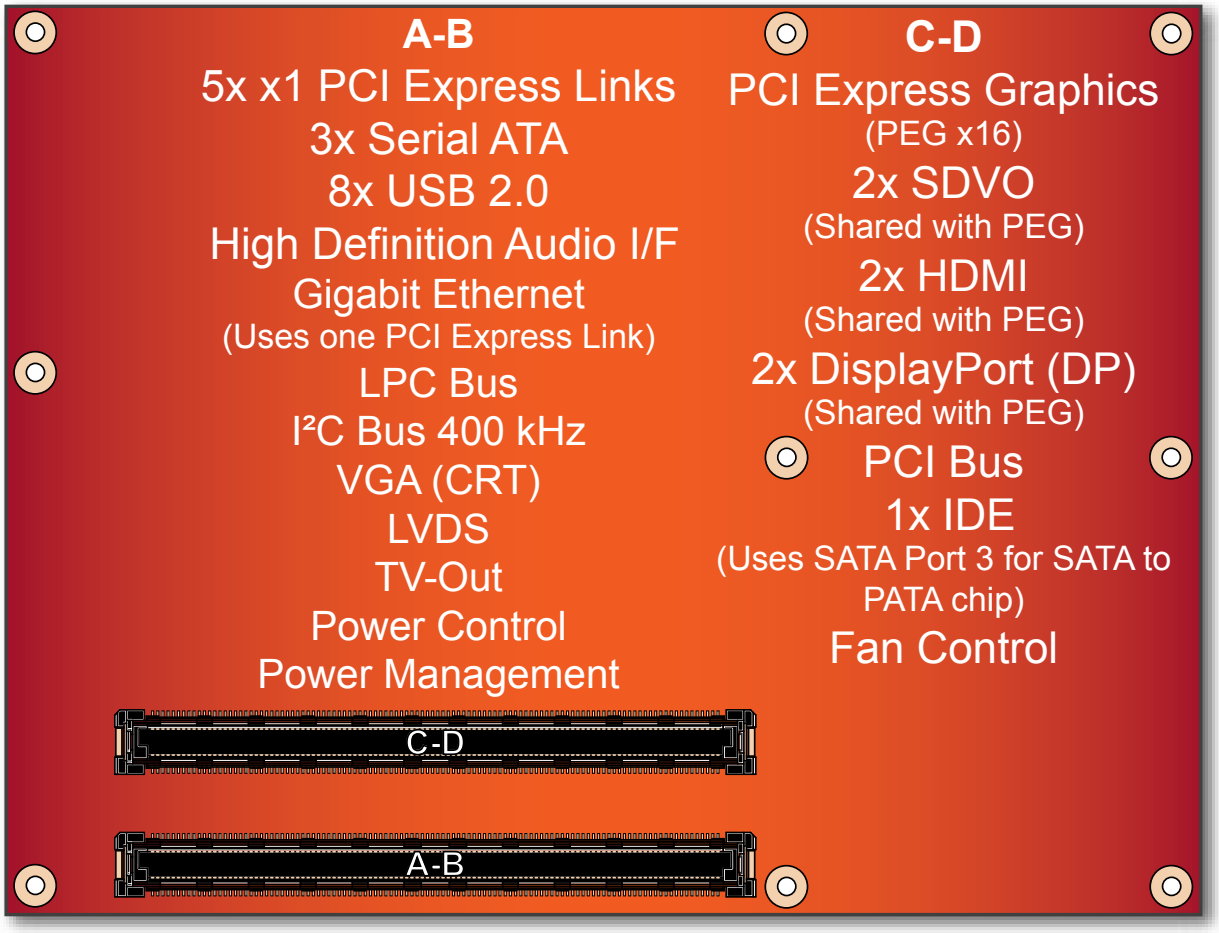


Note

All measurements are in millimeters. Torque specification for heatspreader screws is 0.5 Nm.

4 Connector Subsystems Rows A, B, C, D

The conga-BM45 is connected to the carrier board via two 220-pin connectors (COM Express Type 2 pinout) for a total of 440 pins connectivity. These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.



top view

In this view the connectors are seen “through” the module.

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4.1 Primary Connector Rows A and B

The following subsystems can be found on the primary connector rows A and B.

4.1.1 Serial ATA™ (SATA)

Three Serial ATA connections are provided via the Intel® 82801IEM (ICH9M-E). SATA is an enhancement of the parallel ATA therefore offering higher performance. As a result of this enhancement the traditional restrictions of parallel ATA are overcome with respect to speed and EMI. SATA starts with a transfer rate of 150 Mbytes/s and can be expanded up to 600 Mbytes/s in order to accommodate future developments. SATA is completely protocol and software compatible to parallel ATA. If the conga-BM45 does not support the PATA interface then four Serial ATA connections are available at connector rows A and B. See section 6.2 for more information about the Serial ATA features on the conga-BM45.

4.1.2 USB 2.0

The conga-BM45 offers six UHCI USB host controllers and two EHCI USB host controller provided by the Intel® 82801IEM (ICH9M-E) I/O controller hub. These controllers comply with USB standard 1.1 and 2.0 and offer a total of 8 USB ports via connector rows A and B. Each port is capable of supporting USB 1.1 and 2.0 compliant devices. For more information about how the USB host controllers are routed see section 6.7.

Note

The USB controller is a PCI bus device. The BIOS allocates the necessary system resources when configuring the PCI devices.

4.1.3 High Definition Audio (HDA) Interface

The conga-BM45 provides an interface that supports the connection of HDA audio codecs.

4.1.4 Gigabit Ethernet

The conga-BM45 is equipped with a Gigabit Ethernet Controller that is integrated within the Intel® 82801IEM (ICH9M-E) I/O controller hub. This controller is combined with an Intel® 82567 Phy. that is implemented through the use of the sixth x1 PCI Express link. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board. The Gigabit Ethernet interface supports Intel® Active Management Technology 4.0 (Intel® AMT). For more information about Intel® AMT see section 6.8 ‘Intel® Active Management Technology (Intel® AMT) 4.0 of this document’.

4.1.5 LPC Bus

conga-BM45 offers the LPC (Low Pin Count) bus through the use of the Intel® 82801IEM (ICH9M-E). There are many devices available for this Intel® defined bus. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific baseboard using this bus. See section 8.2.1 for more information about the LPC Bus.

4.1.6 I²C Bus 400kHz

The I²C bus is implemented through the use of ATMEL ATmega168 microcontroller. It provides a Fast Mode (400kHz max.) multi-master I²C Bus that has maximum I²C bandwidth.

4.1.7 PCI Express™

The conga-BM45 offers 6x x1 PCI Express links via the Intel® 82801IEM (ICH9M-E), which can be configured to support PCI Express edge cards or ExpressCards. One of the six x1 PCI Express links is utilized by the onboard Gigabit Ethernet interface therefore there are only 5x x1 PCI Express links available on the A,B connector row.

Additionally, these links can be statically configured as 5 x1 or 1 x4 plus 1 x1. AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1KΩ resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled for channels 0-3. Channel 4 remains configured as a x1 link. The PCI Express interface is based on the PCI Express Specification 1.0a.

4.1.8 ExpressCard™

The conga-BM45 supports the implementation of ExpressCards, which requires the dedication of one USB port and one PCI Express link for each ExpressCard used.

4.1.9 Graphics Output (VGA/CRT)

The conga-BM45 graphics are driven by an Intel® Graphics Media Accelerator 4500MHD engine, which is incorporated into the Intel® GM45 chipset found on the conga-BM45. This graphic engine offers significantly higher performance than previous Intel® graphics engines found on other Intel® chipsets.

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4.1.10 LCD

The Intel® GM45 chipset, found on the conga-BM45, offers an integrated dual channel LVDS interface. There are two LVDS transmitter channels (Channel A and Channel B) in the LVDS interface. Channel A and Channel B consist of 4-data pairs and a clock pair each.

4.1.11 TV-Out

TV-Out support is integrated into the Intel® GM45 chipset. This integrated encoder converts RGB data into various analog television standards (NTSC, PAL) and formats (composite, S-Video) and provides it via the TV-Out port.

4.1.12 Power Control

PWR_OK

Power OK from main power supply. A high value indicates that the power is good. Using this input is optional. Through the use of an internal monitor on the +12V ± 5% input voltage, and/or the internal power supplies, the conga-BM45 module is capable of generating its own power-on reset. According to the COM Express™ Specification PWR_OK is a 3.3V signal.

The conga-BM45 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-BM45's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A-B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the A-B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

12 volt input power is the sole operational power source for the conga-BM45. The remaining necessary voltages are internally generated on

the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-BM45 application:

- It has also been noticed that on some occasions problems occur when using a 12V power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information about this issue visit www.formfactors.org and view page 25 figure 7 of the document "ATX12V Power Supply Design Guide V2.2".

4.1.13 Power Management

APM 1.2 compliant. ACPI 2.0 compliant with battery support. Also supports Suspend to RAM (S3).

4.2 Secondary Connector Rows C and D

The following subsystems can be found on the secondary connector rows C and D.

4.2.1 PCI Express Graphics (PEG)

The conga-BM45 supports the implementation of a x16 link for an external high-performance PCI Express Graphics card. It supports a theoretical bandwidth of up to 4GB/s (unidirectional). Each lane of the PEG Port consists of a receive and transmit differential signal pair designated from PEG_RX0± to PEG_RX15± and correspondingly from PEG_TX0± to PEG_RX15±. It's also possible to utilize a standardized Advanced Digital Display Card 2nd Generation (ADD2-based on SDVO) via the x16 PEG Port connector, which can support a wide variety of display options like DVI, LVDS, TV-Out and HDMI.

It is also possible to optionally use the PEG interface for connecting a x1, x2, x4, or x8 non-graphic PCI Express device instead of using the x16 link for a PCI Express graphics device. This will increase the available PCI Express links on top of those explained in section 4.1.7. These additional links cannot be linked together with each other or with the other PCI Express links found on the conga-BM45.

4.2.2 SDVO

The pins of PEG Port are shared with the Serial Digital Video Ouput (SDVO) functionality and may be alternatively used for two third party SDVO compliant devices connected to channels B and C. See section 7.5 of this document for more information about enabling SDVO peripherals.

4.2.3 HDMI

The Intel® GM45 chipset on the conga-BM45 supports integrated HDMI, which is multiplexed onto the PCI Express Graphics (PEG) interface. The Intel® GM45 provides two ports capable of supporting HDMI. This integrated HDMI solution saves BOM cost compared to HDMI over SDVO. See section 7.5 of this document for more information about enabling HDMI peripherals.

Note

The standard variant of conga-BM45 does not support Intel® HD Audio on either of the HDMI ports. For more information about this subject contact congatec technical support. For more information about implementing a HDMI interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

4.2.4 DisplayPort (DP)

The conga-BM45 offers two DP ports, each capable of supporting link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes. The DP is multiplexed onto the PCI Express Graphics (PEG) interface. The DisplayPort specification is a VESA standard aimed at consolidating internal and external connection methods to reduce device complexity, supporting key cross industry applications, and providing performance scalability to enable the next generation of displays. The Intel® GM45 chipset can support a maximum of 2 DP ports simultaneously.

Note

The standard variant of conga-BM45 does not support Intel® HD Audio on either of the DP ports. For more information about this subject contact congatec technical support. For more information about implementing a DisplayPort interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

4.2.5 PCI Bus

The PCI bus complies with PCI specification Rev. 2.3 and provides a 32bit parallel PCI bus that is capable of operating at 33MHz.

Note

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

4.2.6 IDE (PATA)

The conga-BM45 supports an IDE channel that is capable of UDMA-100 operation. This channel is implemented by converting SATA Port 3 to an IDE channel using JMicron's single chip solution for serial and parallel ATA translation. The IDE interface supports the connection of only one device at any given moment.

5 Additional Features

5.1 Watchdog

The conga-BM45 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express™ Specification does not provide support for external hardware triggering of the Watchdog, which means the conga-BM45 does not support external hardware triggering. For more information about the Watchdog feature see the BIOS setup description section 9.4.13 of this document and application note AN3_Watchdog.pdf on the congatec AG website at www.congatec.com.

5.2 Onboard Microcontroller

The conga-BM45 is equipped with an ATMEL Atmega168 microcontroller. This onboard microcontroller plays an important role for most of the congatec BIOS features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode.

5.3 Embedded BIOS

The conga-BM45 is equipped with congatec Embedded BIOS and has the following features:

- ACPI Power Management
- ACPI Battery Support
- Supports Customer Specific CMOS Defaults
- Multistage Watchdog
- User Data Storage
- Manufacturing Data and Board Information
- OEM Splash Screen
- Flat Panel Auto Detection and Backlight Control
- BIOS Setup Data Backup (see section 5.3.1)
- Exclusive PCI Interrupts
- Fast Mode I²C Bus

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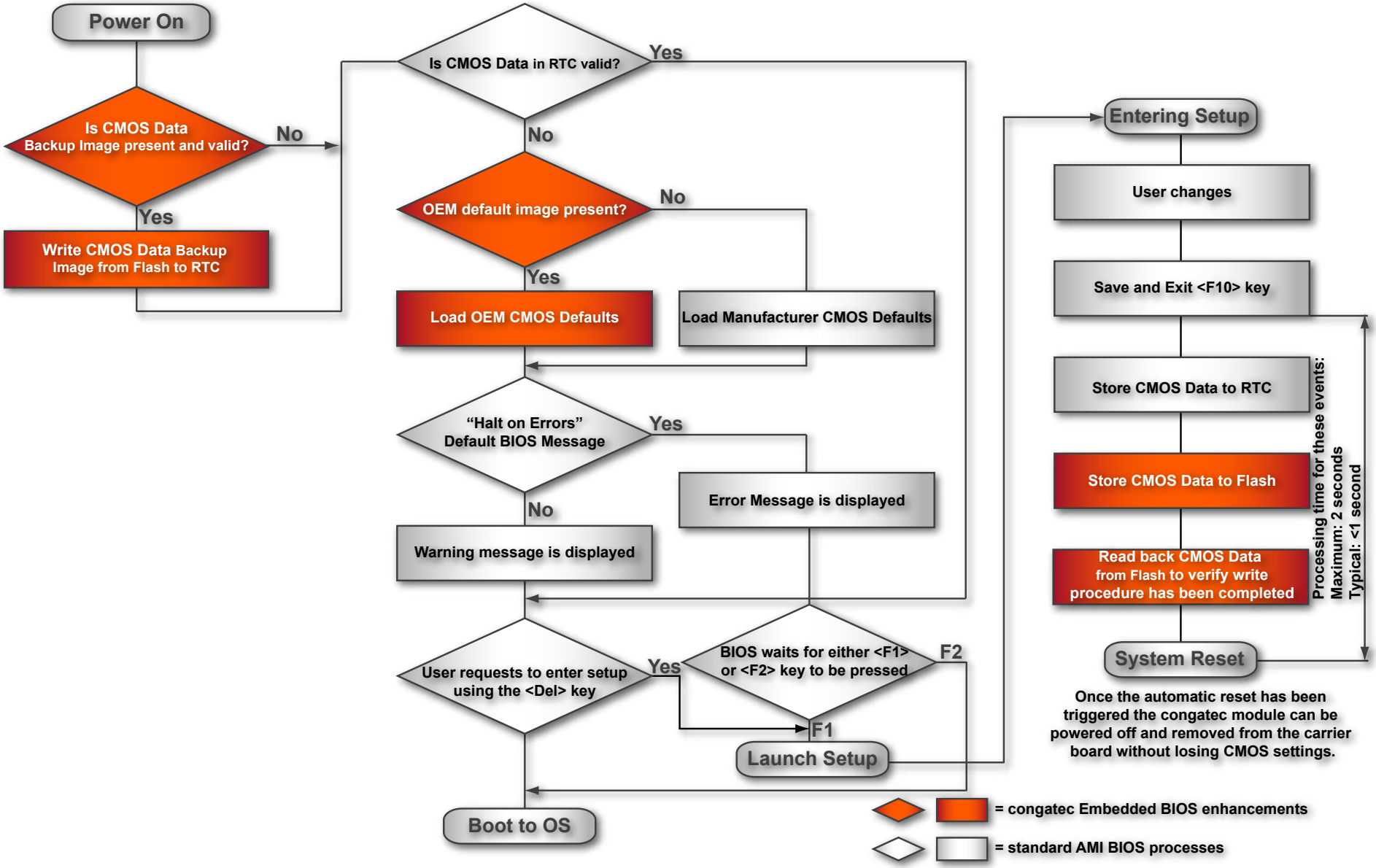
5.3.1 Simplified Overview of BIOS Setup Data Backup


Power On
Is CMOS Data Backup Image present and valid?
No
Yes
Write CMOS Data Backup Image from Flash to RTC
Is CMOS Data in RTC valid?
Yes
No
OEM default image present?
No
Yes
Load OEM CMOS Defaults
Load Manufacturer CMOS Defaults
"Halt on Errors" Default BIOS Message
Yes
Error Message is displayed
No
Warning message is displayed
User requests to enter setup using the <Del> key
Yes
BIOS waits for either <F1> or <F2> key to be pressed
F2
F1
Launch Setup
Boot to OS
Entering Setup
User changes
Save and Exit <F10> key
Store CMOS Data to RTC
Store CMOS Data to Flash
Read back CMOS Data from Flash to verify write procedure has been completed
Processing time for these events:
Maximum: 2 seconds
Typical: <1 second
System Reset
Once the automatic reset has been triggered the congatec module can be powered off and removed from the carrier board without losing CMOS settings.
= congatec Embedded BIOS enhancements
= standard AMI BIOS processes

The above diagram provides an overview of how the BIOS Setup Data is backed up on congatec modules. OEM default values mentioned above refer to customer specific CMOS settings created using the congatec System Utility tool.

Once the BIOS Setup Program has been entered and the settings have been changed, the user saves the settings and exits the BIOS Setup Program using the F10 key feature. After the F10 function has been evoked, the CMOS Data is stored in a dedicated non-volatile CMOS Data Backup area located in the BIOS Flash Memory chip as well as RTC. The CMOS Data is written to and read back from the CMOS Data Backup area and verified. Once verified the F10 Save and Exit function continues to perform some minor processing tasks and finally reaches an automatic reset point, which instructs the module to reboot. After the Automatic Reset has been triggered the congatec module can be powered off and if need be removed from the baseboard without losing the new CMOS settings.

5.4 Security Features

The conga-BM45 can be equipped optionally with a “Trusted Platform Module“ (TPM 1.2). This TPM 1.2 includes coprocessors to calculate efficient hash and RSA algorithms with key lengths up to 2,048 bits as well as a real random number generator. Security sensitive applications like gaming and e-commerce will benefit also with improved authentication, integrity and confidence levels.

5.5 Suspend to Ram

The Suspend to RAM feature is available on the conga-BM45.

5.6 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec AG has defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

The conga-BM45 BIOS fully supports this interface. For more information about this subject visit the congatec website and view the following documents:

- congatec Battery Management Interface Specification
- Battery System Design Guide
- conga-SBMC User’s Guide

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6 conga Tech Notes

The conga-BM45 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features. This information will also help to gain a better understanding of the information found in the System Resources section of this user's guide as well as some of the setup nodes found in the BIOS Setup Program description section.

6.1 Comparison of I/O APIC to 8259 PIC Interrupt mode

I/O APIC (Advanced Programmable Interrupt controller) mode deals with interrupts differently than the 8259 PIC.

The method of interrupt transmission used by APIC mode is implemented by transmitting interrupts through the system bus and they are handled without the requirement of the processor to perform an interrupt acknowledge cycle.

Another difference between I/O APIC and 8259 PIC is the way the interrupt numbers are prioritized. Unlike the 8259 PIC, the I/O APIC interrupt priority is independent of the actual interrupt number.

A major advantage of the I/O APIC found in the chipset of the conga-BM45 is that it's able to provide more interrupts, a total of 24 to be exact. It must be mentioned that the APIC is not supported by all operating systems. In order to utilize the APIC mode it must be enabled in the BIOS setup program before the installation of the OS and it only functions in ACPI mode. You can find more information about APIC in the IA-32 Intel Architecture Software Developer's Manual, Volume 3 in chapter 8.

Note

You must ensure that your operating system supports APIC mode in order to use it.

6.2 Intel® Matrix Storage Technology

The ICH9M-E provides support for Intel® Matrix Storage Technology, providing both AHCI and integrated RAID functionality.

6.2.1 AHCI

The ICH9M-E provides hardware support for Advanced Host Controller Interface (AHCI), a new programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

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6.2.2 RAID

The industry-leading RAID capability provides high performance RAID 0, 1, 5, and 10 functionality on the 4 SATA ports of ICH9M-E. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft* Windows* compatible driver, and a user interface for configuration and management of the RAID capability of ICH9M-E.

For more information about RAID support on the conga-BM45 refer to application note AN15_Configure_RAID_System.pdf, which can be found on the congatec AG website at www.congatec.com.

6.3 Native vs. Compatible IDE mode

6.3.1 Compatible Mode

When operating in compatible mode, SATA controller 1 needs two legacy IRQs (14 and 15) and is unable to share these IRQs with other devices. This is a result of the fact that SATA controller 1 emulates the primary and secondary legacy IDE controllers. SATA controller 2 does not support compatible mode.

6.3.2 Native Mode

Native mode allows the SATA controllers to operate as true PCI devices and therefore do not need dedicated legacy resources, which means they can be configured anywhere within the system. When either SATA controller 1 or 2 runs in native mode it only requires one PCI interrupt for both channels and also has the ability to share this interrupt with other devices in the system. Setting Enhanced mode in the BIOS setup program will automatically enable Native mode as Native mode is a subset of Enhanced mode. See section 9.4.8 for more information about this.

Running in native mode frees up interrupt resources (IRQs 14 and 15) and decreases the chance that there may be a shortage of interrupts when installing devices.

Note

If your operating system supports native mode then congatec AG recommends you enable it.

6.4 Intel® Processor Features

6.4.1 Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ 2 Duo and Celeron processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature, that the Intel® Thermal Monitor uses to activate the TCC, cannot be configured by the user nor is it software visible.

The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel Speedstep transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

Note

The maximum operating temperature for Intel® Core™ 2 Duo and Celeron processors is 100°C. TM2 mode is used for Intel® Core™ 2 Duo processors, it is not supported by Intel® Celeron processors.

Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

Note

To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ 2 Duo and Celeron processor's respective datasheet can provide you with more information about this subject.

THERMTRIP# signal is used by Intel®'s Core™ 2 Duo and Celeron processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX style power supply.

6.4.2 Processor Performance Control

Intel® Core™ 2 Duo processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it's not being fully utilized. The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime.

The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

Note

If the "Home/Office" or "Always On" power scheme is selected when using Windows operating systems then the processor will always run at the highest performance state. For more information about this subject see chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info . Also visit Microsoft's website and search for the document called "Windows Native Processor Performance Control".

Celeron processors do not support Enhanced Intel® SpeedStep® technology. They always run at a fixed frequency.

6.4.3 Intel® 64

The formerly known Intel® Extended Memory 64 Technology is an enhancement to Intel®'s IA-32 architecture. Intel® 64 is only available on Core™ 2 Duo processors and is designed to run newly written 64-bit code and access more than 4GB of memory. Processors with Intel® 64 architecture support 64-bit-capable operating systems from Microsoft, Red Hat and SuSE. Processors running in legacy mode remain fully compatible with today's existing 32-bit applications and operating systems

Platforms with Intel® 64 can be run in three basic ways :

1. **Legacy Mode:** 32-bit operating system and 32-bit applications. In this mode no software changes are required, however the benefits of Intel® 64 are not utilized.

2. **Compatibility Mode:** 64-bit operating system and 32-bit applications. This mode requires all device drivers to be 64-bit. The operating system will see the 64-bit extensions but the 32-bit application will not. Existing 32-bit applications do not need to be recompiled and may or may not benefit from the 64-bit extensions. The application will likely need to be re-certified by the vendor to run on the new 64-bit extended operating system.

3. **64-bit Mode:** 64-bit operating system and 64-bit applications. This usage requires 64-bit device drivers. It also requires applications to be modified for 64-bit operation and then recompiled and validated.

Intel® 64 provides support for:

- 64-bit flat virtual address space
- 64-bit pointers
- 64-bit wide general purpose registers
- 64-bit integer support
- Up to one Terabyte (TB) of platform address space

You can find more information about Intel® 64 Technology at: http://developer.intel.com/technology/intel64/index.htm

Note

congatec does not intend to offer BSPs for 64-bit operating systems. Contact congatec technical support if you plan to use a 64-bit operating system on the conga-BM45.

6.4.4 Intel® Virtualization Technology

Virtualization solutions enhanced by Intel® VT will allow a Core™ 2 Duo platform to run multiple operating systems and applications in independent partitions. When using virtualization capabilities, one computer system can function as multiple “virtual” systems. With processor and I/O enhancements to Intel®’s various platforms, Intel® Virtualization Technology can improve the performance and robustness of today’s software-only virtual machine solutions.

Intel® VT is a multi-generational series of extensions to Intel® processor and platform architecture that provides a new hardware foundation for virtualization, establishing a common infrastructure for all classes of Intel® based systems. The broad availability of Intel® VT makes it possible to create entirely new applications for virtualization in servers, clients as well as embedded systems thus providing new ways to improve system reliability, manageability, security, and real-time quality of service.

The success of any new hardware architecture is highly dependent on the system software that puts its new features to use. In the case of virtualization technology, that support comes from the virtual machine monitor (VMM), a layer of software that controls the underlying physical platform resources sharing them between multiple “guest” operating systems. Intel® VT is already incorporated into most commercial and open-source VMMs including those from VMware, Microsoft, XenSource, Parallels, Virtual Iron, Jaluna and TenAsys.

You can find more information about Intel Virtualization Technology at: http://developer.intel.com/technology/virtualization/index.htm

Note

congatec does not offer virtual machine monitor (VMM) software. All VMM software support questions and queries should be directed to the VMM software vendor and not congatec technical support.

6.5 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system’s thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-BM45 ACPI thermal solution offers three different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.

$$\Delta P[\%] = TC1(T_n - T_{n-1}) + TC2(T_n - T_t)$$

- *ΔP is the performance delta*
- *T_t is the target temperature = critical trip point*
- *The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants. These constants are set to fixed values for the conga-BM45:*
- *TC1= 1*
- *TC2= 5*
- *TSP= 5 seconds*

See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

6.6 ACPI Suspend Modes and Resume Events

conga-BM45 supports the S1 (POS= Power On Suspend) state and S3 (STR= Suspend to RAM). For more information about S3 wake events see section 9.4.1 “ACPI Configuration Submenu”.

S4 (Suspend to Disk) is not supported by the BIOS (S4_BIOS) but it is supported by the following operating systems (S4_OS= Hibernate):

- Win2K and WinXP

This table lists the “Wake Events” that resume the system from both S1 or S3 unless otherwise stated in the “Conditions/Remarks” column:

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S1-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
SMBALERT#	Wakes unconditionally from S1-S5.
PCI Express WAKE#	Wakes unconditionally from S1-S3.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S1, no special action must be taken for a USB Mouse/Keyboard Event to be used as a Wake Event. When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event.. USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu. Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: “USBBIOSx“=DWORD:00000000 *Note that Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.* Configure USB keyboard/mouse to be able to wake up the system: In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check ‘Allow this device to bring the computer out of standby’. *Note: When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the above registry entry and rebooting to allow the registry changes to take affect.*
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu.
Watchdog Power Button Event	Wakes unconditionally from S1-S5.

Note

The above list has been verified using a Windows XP SP2 ACPI enabled installation.

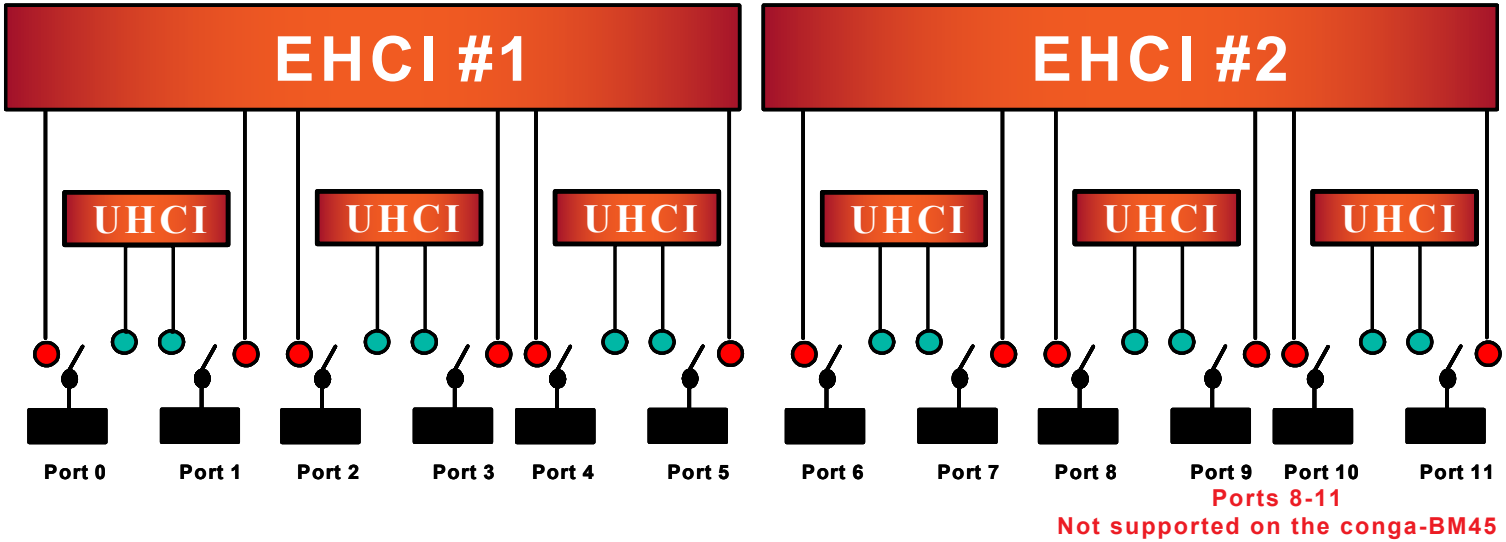
When using Windows XP, Standby mode is either an S1 state or S3 state depending on what has been selected in the ACPI Configuration Menu in the BIOS setup program. For more information about this see section 9.4.1 of this document.

6.7 USB 2.0 EHCI Host Controller Support

The 8 available USB ports are shared between 2 EHCI host controller and the 6 UHCI host controllers.

Within the EHC functionality there is a port-routing logic that executes the mixing between the two different types of host controllers (EHCI and UHCI). This means that when a USB device is connected the routing logic determines who owns the port. If the device is not USB 2.0 compliant, or if the software drivers for EHCI support are not installed, then the UHCI controller owns the ports.

Routing Diagram



6.8 Intel® Active Management Technology (Intel® AMT) 4.0

The conga-BM45 supports Intel® Active Management Technology 4.0 (Intel® AMT) with both wired and wireless LAN support via a Controller Link interface from the Intel® GM45 to the Intel® I/O Controller Hub 82801IEM (ICH9M-E) for extended manageability functionality. An Intel AMT engine integrated within the Intel® GM45 chipset combines hardware and software solutions to provide:

- Remote Asset Management
- Remote Diagnosis and Repair
- Remote Agent Presence
- Wireless OOB Management
- Circuit Breaker Network Isolation
- Mobile Power Management Policies
- 3rd Party Non-Volatile Storage

Note

For more information about Intel® Active Management Technology (Intel® AMT) 4.0 visit the Intel® website.

7 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express™ Type II connectors used for congatec AG modules.

Table 2 describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express™ module pull-up or pull-down resistor has been used, if the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip’s datasheet.

Table 2 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 1.0a
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

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7.1 A-B Connector Signal Descriptions

Table 3 Intel® High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
AC_RST#	A30	**Intel® High Definition Audio Reset:** This signal is the master hardware reset to external codec(s).	O 3.3V		AC'97 codecs are not supported.
AC_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC'97 codecs are not supported. AC_SYNC is a boot strap signal (see note below)
AC_BITCLK	A32	**Intel® High Definition Audio Bit Clock Output:** This signal is a 24.000MHz serial data clock generated by the Intel® High Definition Audio controller (the Intel® ICH9M-E). This signal has an Intel® integrated pull-down resistor so that AC_BIT_CLK doesn't float when an Intel® High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.	I 3.3V O 3.3V		AC'97 codecs are not supported.
AC_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC'97 codecs are not supported. AC_SDOUT is a boot strap signal (see note below)
AC_SDIN[2:0]	B28-B30	**Intel® High Definition Audio Serial Data In [0]:** These signals are serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I 3.3V		AC'97 codecs are not supported.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module.

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1KΩ resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled for channels 0-3. x1 mode is used by default if these resistors are not populated. Channel 4 remains configured as x1 mode regardless of the configuration of channels 0-3.

For more information refer to section 7.5 of this user's guide.

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Table 4 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Some pairs are unused in some modes according to the following: 1000 / 100 / 10 MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	I/O Analog		Twisted pair signals for external transformer.
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.	OD		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	OD		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	OD		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.	REF		Reference voltage on conga-BM45 is 1.8V

Table 5 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 1.0a. Serial ATA channel 3 is used for SATA to PATA conversion and therefore not available.
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 1.0a. Serial ATA channel 3 is used for SATA to PATA conversion and therefore not available.
ATA_ACT#	A28	ATA (parallel and serial) or SAS activity indicator, active low.	OC 3.3V		

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Table 6 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 1.1
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair.	I PCIE		Not available. Used by onboard Gigabit Ethernet.
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair.	O PCIE		Not available. Used by onboard Gigabit Ethernet.
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		

Note

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1KΩ resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled for channels 0-3. x1 mode is used by default if these resistors are not populated. Channel 4 remains configured as x1 mode regardless of the configuration of channels 0-3.

For more information refer to section 7.5 of this user's guide.

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Table 7 ExpressCard Support Pins Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
EXCD0_CPPE# EXCD1_CPPE#	A49 B48	ExpressCard capable card request.	I 3.3V	PU 10k 3.3V	
EXCD0_PERST# EXCD1_PERST#	A48 B47	ExpressCard Reset	O 3.3V	PU 10k 3.3V	EXCD0_PERST# is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 8 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC multiplexed address, command and data bus	I/O 3.3V		
LPC_FRAME#	B3	LPC frame indicates the start of an LPC cycle	O 3.3V		
LPC_DRQ[0:1]#	B8-B9	LPC serial DMA request	I 3.3V		
LPC_SERIRQ	A50	LPC serial interrupt	I/O 3.3V	PU 10k 3.3V	
LPC_CLK	B10	LPC clock output - 33MHz nominal	O 3.3V		

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Table 9 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	USB Port 0, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB0-	A45	USB Port 0, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+	B46	USB Port 1, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1-	B45	USB Port 1, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+	A43	USB Port 2, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2-	A42	USB Port 2, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+	B43	USB Port 3, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3-	B42	USB Port 3, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+	A40	USB Port 4, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4-	A39	USB Port 4, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+	B40	USB Port 5, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5-	B39	USB Port 5, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+	A37	USB Port 6, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6-	A36	USB Port 6, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+	B37	USB Port 7, data + or D+	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7-	B36	USB Port 7, data - or D-	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low. .	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.

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Table 10 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_GRN	B91	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	O Analog	PD 150R	Analog output
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O 5V	PU 2k2 3.3V	
VGA_I2C_DAT	B96	DDC data line.	I/O 5V	PU 2k2 3.3V	

Table 11 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	A71 A72 A73 A74 A75 A76 A78 A79	LVDS Channel A differential pairs	O LVDS		
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	B71 B72 B73 B74 B75 B76 B77 B78	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS Channel B differential clock	O LVDS		
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3V	PD 10k	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3V		
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control.	O 3.3V	PU 2k2 3.3V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control.	I/O 3.3V	PU 2k2 3.3V	

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Table 12 TV-Out Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TV_DAC_A	B97	TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used	O Analog	PD 150R	Analog output
TV_DAC_B	B98	TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal. S-Video: Luminance analog signal.	O Analog	PD 150R	Analog output
TV_DAC_C	B99	TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal.	O Analog	PD 150R	Analog output

Table 13 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/O 3.3V	PU 4k7 3.3V	
I2C_DAT	B34	General purpose I²C port data I/O line	I/O 3.3V	PU 4k7 3.3V	
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPEAKER is a boot strap signal (see note below)
BIOS_DISABLE#	A34	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.	I 3.3V	PU 10k 3.3V	
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PU 10k 3.3V	
KBD_RST#	A86	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	I	PU 10k 3.3V	
KBD_A20GATE	A87	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.	I	PU 10k 3.3V	

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user’s guide.

Table 14 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO[0]	A93	General purpose output pins.	O 3.3VSB	PU 10k 3.3VSB	
GPO[1]	B54	General purpose output pins.	O 3.3VSB	PU 10k 3.3VSB	
GPO[2]	B57	General purpose output pins.	O 3.3VSB	PU 10k 3.3VSB	
GPO[3]	B63	General purpose output pins.	O 3.3VSB	PU 10k 3.3VSB	
GPI[0]	A54	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[1]	A63	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[2]	A67	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	
GPI[3]	A85	General purpose input pins. Pulled high internally on the module.	I 3.3VSB	PU 10k 3.3VSB	

Table 15 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on rising edge.	I 3.3VSB	PU 10k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10k 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3V	PD 100k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V		Set by resistor divider to accept 3.3V.
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as “PS_ON”) may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PU 10k 3.3VSB	
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output.	O 3.3VSB	PU 10k 3.3VSB	Not supported
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PU 10k 3.3VSB	
WAKE0#	B66	PCI Express wake up signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement wake-up on PS/2 keyboard or mouse activity.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3VSB	PU 8k2 3.3VSB	
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation.	I 3.3V	PU 8k2 3.3V	
THERMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3V	PU 10k 3.3V	
SMB_CK	B13	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	I/O 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	I 3.3VSB	PU 10k 3.3VSB	

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Table 16 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A97-A99 A101-A109 B101-B109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A66, A80, A90, A96, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

7.2 A-B Connector Pinout

Table 17 Connector A-B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF (*)	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4# (*)	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+

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Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	ATA_ACT#	B28	AC_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC_SYNC	B29	AC_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC_RST#	B30	AC_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	KBD_RST#	B86	VCC_5V_SBY
A32	AC_BITCLK	B32	SPKR	A87	KBD_A20GATE	B87	VCC_5V_SBY
A33	AC_SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	RSVD
A34	BIOS_DISABLE#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	RSVD	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	RSVD	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	RSVD	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	RSVD	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	GND	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	VCC_12V	B97	TV_DAC_A
A43	USB2+	B43	USB3+	A98	VCC_12V	B98	TV_DAC_B
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	VCC_12V	B99	TV_DAC_C
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	VCC_12V	B101	VCC_12V
A47	VCC_RTC	B47	EXCD1_PERST#	A102	VCC_12V	B102	VCC_12V
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	VCC_12V	B103	VCC_12V
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-BM45. PCIE_TX5± and PCIE_RX5± are used for the onboard Gigabit Ethernet and therefore are not available externally. SATA3_TX+, SATA3_TX-, SATA3_RX+, and SATA3_RX- are used for SATA to PATA conversion and therefore not available externally.

7.3 C-D Connector Signal Descriptions

Table 18 PCI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_AD[0, 2, 4, 6, 8, 10, 12] PCI_AD[1, 3, 5, 7] PCI_AD[9, 11, 13, 15] PCI_AD14 PCI_AD[16, 18, 20, 22] PCI_AD[17, 19] PCI_AD[21, 23] PCI_AD[24, 26, 28, 30] PCI_AD[25, 27, 29, 31]	C24-C30 D22-D25 D27-D30 C32 D37-D40 C39-C40 C42-C43 D42-D45 C45-C48	PCI bus multiplexed address and data lines	I/O 3.3V		
PCI_C/BE0# PCI_C/BE1# PCI_C/BE2# PCI_C/BE3#	D26 C33 C38 C44	PCI bus byte enable lines, active low	I/O 3.3V		
PCI_DEVSEL#	C36	PCI bus Device Select, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_FRAME#	D36	PCI bus Frame control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_STOP#	D34	PCI bus STOP control line, active low, driven by cycle initiator.	I/O 3.3V	PU 8k2 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V		
PCI_PERR#	C34	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	I/O 3.3V	PU 8k2 3.3V	
PCI_REQ0# PCI_REQ1# PCI_REQ2# PCI_REQ3#	C22 C19 C17 D20	PCI bus master request input lines, active low.	I 3.3V	PU 8k2 3.3V	
PCI_GNT0# PCI_GNT1# PCI_GNT2# PCI_GNT3#	C20 C18 C16 D19	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT[0..3]# are boot strap signals (see note below)
PCI_RESET#	C23	PCI Reset output, active low.	O 3.3V		
PCI_LOCK#	C35	PCI Lock control line, active low.	I/O 3.3V	PU 8k2 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	I/O 3.3V	PU 8k2 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	I 3.3VSB		

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Signal	Pin #	Description	I/O	PU/PD	Comment
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	PU 10k 3.3V	
PCI_IRQA# PCI_IRQB# PCI_IRQC# PCI_IRQD#	C49 C50 D46 D47	PCI interrupt request lines.	I 3.3V	PU 8k2 3.3V	
PCI_CLK	D50	PCI 33MHz clock output.	O 3.3V		
PCI_M66EN	D49	Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66MHz operation. If the module is not capable of supporting 66MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33MHz.	I		Not connected

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

The PCI interface is specified to be +5V tolerant, with +3.3V signaling.

Table 19 IDE Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IDE_D0 IDE_D1 IDE_D2 IDE_D3 IDE_D4 IDE_D5 IDE_D6 IDE_D7 IDE_D8 IDE_D9 IDE_D10 IDE_D11 IDE_D12 IDE_D13 IDE_D14 IDE_D15	D7 C10 C8 C4 D6 D2 C3 C2 C6 C7 D3 D4 D5 C9 C12 C5	Bidirectional data to / from IDE device.	I/O 3.3V	IDE_D7 PD 10k	
IDE_A[0.2]	D13-D15	Address lines to IDE device.	O 3.3V		
IDE_IOW#	D9	I/O write line to IDE device. Data latched on trailing (rising) edge.	O 3.3V		
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V		
IDE_REQ	D8	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	I 3.3V	PD 5k1	
IDE_ACK#	D10	IDE Device DMA Acknowledge.	O 3.3V		
IDE_CS1#	D16	IDE Device Chip Select for 1F0h to 1FFh range.	O 3.3V		
IDE_CS3#	D17	IDE Device Chip Select for 3F0h to 3FFh range.	O 3.3V		
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	I 3.3V	PU 4k7 3.3V	
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V		
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V	PD 10k	
IDE_CBLID#	D77	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	I 3.3V	PD 1k	

Note

The PATA (IDE) interface is an option conga-BM45. When this option is used, Serial ATA channel 3 is not available.

Table 20 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+	C52	PCI Express Graphics Receive Input differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Receive Input differential pairs 16 through 31 known as PCIE_RX[16-31] + and -.*	I PCIE		
PEG_RX0-	C53				
PEG_RX1+	C55				
PEG_RX1-	C56				
PEG_RX2+	C58				
PEG_RX2-	C59				
PEG_RX3+	C61				
PEG_RX3-	C62				
PEG_RX4+	C65				
PEG_RX4-	C66				
PEG_RX5+	C68				
PEG_RX5-	C69				
PEG_RX6+	C71				
PEG_RX6-	C72				
PEG_RX7+	C74				
PEG_RX7-	C75				
PEG_RX8+	C78				
PEG_RX8-	C79				
PEG_RX9+	C81				
PEG_RX9-	C82				
PEG_RX10+	C85				
PEG_RX10-	C86				
PEG_RX11+	C88				
PEG_RX11-	C89				
PEG_RX12+	C91				
PEG_RX12-	C92				
PEG_RX13+	C94				
PEG_RX13-	C95				
PEG_RX14+	C98				
PEG_RX14-	C99				
PEG_RX15+	C101				
PEG_RX15-	C102				

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Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_TX0+ PEG_TX0- PEG_TX1+ PEG_TX1- PEG_TX2+ PEG_TX2- PEG_TX3+ PEG_TX3- PEG_TX4+ PEG_TX4- PEG_TX5+ PEG_TX5- PEG_TX6+ PEG_TX6- PEG_TX7+ PEG_TX7- PEG_TX8+ PEG_TX8- PEG_TX9+ PEG_TX9- PEG_TX10+ PEG_TX10- PEG_TX11+ PEG_TX11- PEG_TX12+ PEG_TX12- PEG_TX13+ PEG_TX13- PEG_TX14+ PEG_TX14- PEG_TX15+ PEG_TX15-	D52 D53 D55 D56 D58 D57 D61 D62 D65 D66 D68 D69 D71 D72 D74 D75 D78 D79 D81 D82 D85 D86 D88 D89 D91 D92 D94 D95 D98 D99 D101 D102	PCI Express Graphics Transmit Output differential pairs. Some of these lines are multiplexed with SDVO lines. *Note: Can also be used as PCI Express Transmit Output differential pairs 16 through 31 known as PCIE_TX[16-31] + and -.*	O PCIE		
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	I 1.05V		PEG_LANE_RV# is a boot strap signal (see note below)
PEG_ENABLE#	D97	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	I 3.3V	PU 10k 3.3V	

It is also possible to optionally use the PEG interface for connecting a x1, x2, x4, or x8 non-graphic PCI Express device instead of using the x16 link for a PCI Express graphics device. This will increase the available PCI Express links on top of those explained in section 4.1.7. These additional links cannot be linked together with each other or with the other PCI Express links found on the conga-BM45.

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more

information refer to section 7.5 of this user's guide.

Table 21 SDVO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDVOB_RED+ SDVOB_RED-	D52 D53	Serial Digital Video B red output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
SDVOB_GRN+ SDVOB_GRN-	D55 D56	Serial Digital Video B green output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
SDVOB_BLU+ SDVOB_BLU-	D58 D59	Serial Digital Video B blue output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
SDVOB_CK+ SDVOB_CK-	D61 D62	Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-.	O PCIE		
SDVOB_INT+ SDVOB_INT-	C55 C56	Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-.	I PCIE		
SDVOC_RED+ SDVOC_RED-	D65 D66	Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		
SDVOC_GRN+ SDVOC_GRN-	D68 D69	Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		
SDVOC_BLU+ SDVOC_BLU-	D71 D72	Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		
SDVOC_CK+ SDVOC_CK-	D74 D75	Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-.	O PCIE		
SDVOC_INT+ SDVOC_INT-	C68 C69	Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-.	I PCIE		
SDVO_TVCLKIN+ SDVO_TVCLKIN-	C52 C53	Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-.	I PCIE		
SDVO_FLDSTALL+ SDVO_FLDSTALL-	C58 C59	Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-.	I PCIE		
SDVO_I2C_CK (SDVO_CLK)	D73	SDVO I²C clock line to set up SDVO peripherals.	O 2.5V		
SDVO_I2C_DAT (SDVO_DATA)	C73	SDVO I²C data line to set up SDVO peripherals.	I/O OD 2.5V		SDVO_I2C_DAT is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 22 HDMI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS_B_CLK + TMDS_B_CLK -	D61 D62	HDMI Port B Clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		
TMDS_B_DATA0+ TMDS_B_DATA0-	D58 D59	HDMI Port B Data0 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]-.	O PCIE		
TMDS_B_DATA1+ TMDS_B_DATA1-	D55 D56	HDMI Port B Data1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]-.	O PCIE		
TMDS_B_DATA2+ TMDS_B_DATA2-	D52 D53	HDMI Port B Data2 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]-.	O PCIE		
TMDS_B_HPD#	C61	HDMI Port B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		
DDPB_CTRLCLK	D73	HDMI port B Control Clock	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_CK (SDVO_CLK)
DDPB_CTRLDATA	C73	HDMI port B Control Data	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_DAT (SDVO_DATA) DDPB_CTRLDATA is a boot strap signal (see note below)
TMDS_C_CLK + TMDS_C_CLK -	D74 D75	HDMI Port C Clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		
TMDS_C_DATA0+ TMDS_C_DATA0-	D71 D72	HDMI Port C Data0 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-.	O PCIE		
TMDS_C_DATA1+ TMDS_C_DATA1-	D68 D69	HDMI Port C Data1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-.	O PCIE		
TMDS_C_DATA2+ TMDS_C_DATA2-	D65 D66	HDMI Port C Data2 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-.	O PCIE		
TMDS_C_HPD#	C74	HDMI Port C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		
DDPC_CTRLCLK	D63	HDMI port C Control Clock	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM45. Therefore congatec has used the reserved (RSVD) pin D63 for this signal.
DDPC_CTRLDATA	D64	HDMI port C Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but is mandatory to support the HDMI interface on conga-BM45. Therefore congatec has used the reserved (RSVD) pin D64 for this signal. DDPC_CTRLDATA is a boot strap signal (see note below)

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 23 DisplayPort (DP) Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DPB_LANE3+ DPB_LANE3-	D61 D62	DisplayPort B Lane3 output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]- pair.	O PCIE		
DPB_LANE2+ DPB_LANE2-	D58 D59	DisplayPort B Lane2 output differential pair. Multiplexed with PEG_TX[2]+ and PEG_TX[2]- pair.	O PCIE		
DPB_LANE1+ DPB_LANE1-	D55 D56	DisplayPort B Lane1 output differential pair. Multiplexed with PEG_TX[1]+ and PEG_TX[1]- pair.	O PCIE		
DPB_LANE0+ DPB_LANE0-	D52 D53	DisplayPort B Lane0 output differential pair. Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair.	O PCIE		
DPB_HPD#	C61	DisplayPort B Hot-plug detect. Multiplexed with PEG_RX[3]+.	I PCIE		
DPB_AUX+ DPB_AUX-	C58 C59	DisplayPort B Aux input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]- pair.	I PCIE		
DDPB_CTRLDATA	C73	Digital Display port B Control Data	I/O OD 3.3V		This signal is multiplexed with SDVO_I2C_DAT (SDVO_DATA). This signal is not used on the DisplayPort interface but it must be used to enable the DisplayPort interface. DDPB_CTRLDATA is a boot strap signal (see note below)
DPC_LANE3+ DPC_LANE3-	D74 D75	DisplayPort C Lane3 output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]- pair.	O PCIE		
DPC_LANE2+ DPC_LANE2-	D71 D72	DisplayPort C Lane2 output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]- pair.	O PCIE		
DPC_LANE1+ DPC_LANE1-	D68 D69	DisplayPort C Lane1 output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]- pair.	O PCIE		
DPC_LANE0+ DPC_LANE0-	D65 D66	DisplayPort C Lane0 output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]- pair.	O PCIE		
DPC_HPD#	C74	DisplayPort C Hot-plug detect. Multiplexed with PEG_RX[7]+.	I PCIE		
DPC_AUX+ DPC_AUX-	C71 C72	DisplayPort C Aux input differential pair. Multiplexed with PEG_RX[6]+ and PEG_RX[6]- pair.	I PCIE		
DDPC_CTRLDATA	D64	Digital Display port C Control Data	I/O OD 3.3V		This signal is not supported by COM Express standard but mandatory to support the DisplayPort interface on conga-BM45. Therefore congatec has used the reserved (RSVD) pin D64 for this signal. This signal is not used on the DisplayPort interface but it must be used to enable the DisplayPort interface. DDPC_ CTRLDATA is a boot strap signal (see note below)
DPD_LANE3+ DPD_LANE3-	D88 D89	DisplayPort D Lane3 output differential pair. Multiplexed with PEG_TX[11]+ and PEG_TX[11]- pair.	O PCIE		Not supported
DPD_LANE2+ DPD_LANE2-	D85 D86	DisplayPort D Lane2 output differential pair. Multiplexed with PEG_TX[10]+ and PEG_TX[10]- pair.	O PCIE		Not supported
DPD_LANE1+ DPD_LANE1-	D81 D82	DisplayPort D Lane1 output differential pair. Multiplexed with PEG_TX[9]+ and PEG_TX[9]- pair.	O PCIE		Not supported
DPD_LANE0+ DPD_LANE0-	D78 D79	DisplayPort D Lane0 output differential pair. Multiplexed with PEG_TX[8]+ and PEG_TX[8]- pair.	O PCIE		Not supported

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Signal	Pin #	Description	I/O	PU/PD	Comment
DPD_HPD#	C88	DisplayPort D Hot-plug detect. Multiplexed with PEG_RX[11]+.	I PCIE		Not supported
DPD_AUX+ DPD_AUX-	C85 C86	DisplayPort D Aux input differential pair. Multiplexed with PEG_RX[10]+ and PEG_RX[10]- pair.	I PCIE		Not supported

Note

Some signals have special functionality during the reset process. They may bootstrap some basic important functions of the module. For more information refer to section 7.5 of this user's guide.

Table 24 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	Comment
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pinout Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pinout Type 1 NC NC NC Pinout Type 2 NC NC GND Pinout Type 3 (no IDE) NC GND NC Pinout Type 4 (no PCI) NC GND GND Pinout Type 5 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	PDS	TYPE[0:2]# signals are available on all modules following the Type 2-5 Pinout standard. The conga-BM45 is based on the COM Express Type 2 pinout therefore these pins are not connected.

Table 25 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
GND	C1, C11, C21, C31, C41, C51, C60, C70, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D11, D21, D31, D41, D51, D60, D67, D70, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

Table 26 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FAN_PWMOUT	C67	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD		
FAN_TACHOIN	C77	Fan tachometer input.	I OD		Requires a fan with a two pulse output.
PP_TPM	C83	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V		Trusted Platform Module chip is optional.

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7.4 C-D Connector Pinout

Table 27 Connector C-D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	IDE_D7	D2	IDE_D5	C57	TYPE1#	D57	TYPE2#
C3	IDE_D6	D3	IDE_D10	C58	PEG_RX2+	D58	PEG_TX2+
C4	IDE_D3	D4	IDE_D11	C59	PEG_RX2-	D59	PEG_TX2-
C5	IDE_D15	D5	IDE_D12	C60	GND (FIXED)	D60	GND (FIXED)
C6	IDE_D8	D6	IDE_D4	C61	PEG_RX3+	D61	PEG_TX3+
C7	IDE_D9	D7	IDE_D0	C62	PEG_RX3-	D62	PEG_TX3-
C8	IDE_D2	D8	IDE_REQ	C63	RSVD	D63	DDPC_CTRLCLK
C9	IDE_D13	D9	IDE_IOW#	C64	RSVD	D64	DDPC_CTRLDATA
C10	IDE_D1	D10	IDE_ACK#	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	IDE_D14	D12	IDE_IRQ	C67	FAN_PWMOUT	D67	GND
C13	IDE_IORDY	D13	IDE_A0	C68	PEG_RX5+	D68	PEG_TX5+
C14	IDE_IOR#	D14	IDE_A1	C69	PEG_RX5-	D69	PEG_TX5-
C15	PCI_PME#	D15	IDE_A2	C70	GND (FIXED)	D70	GND (FIXED)
C16	PCI_GNT2#	D16	IDE_CS1#	C71	PEG_RX6+	D71	PEG_TX6+
C17	PCI_REQ2#	D17	IDE_CS3#	C72	PEG_RX6-	D72	PEG_TX6-
C18	PCI_GNT1#	D18	IDE_RESET#	C73	SDVO_DATA	D73	SVDO_CLK
C19	PCI_REQ1#	D19	PCI_GNT3#	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCI_GNT0#	D20	PCI_REQ3#	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCI_REQ0#	D22	PCI_AD1	C77	FAN_TACHOIN	D77	IDE_CBLID#
C23	PCI_RESET#	D23	PCI_AD3	C78	PEG_RX8+	D78	PEG_TX8+
C24	PCI_AD0	D24	PCI_AD5	C79	PEG_RX8-	D79	PEG_TX8-
C25	PCI_AD2	D25	PCI_AD7	C80	GND (FIXED)	D80	GND (FIXED)
C26	PCI_AD4	D26	PCI_C/BE0#	C81	PEG_RX9+	D81	PEG_TX9+
C27	PCI_AD6	D27	PCI_AD9	C82	PEG_RX9-	D82	PEG_TX9-
C28	PCI_AD8	D28	PCI_AD11	C83	PP_TPM	D83	RSVD
C29	PCI_AD10	D29	PCI_AD13	C84	GND	D84	GND
C30	PCI_AD12	D30	PCI_AD15	C85	PEG_RX10+	D85	PEG_TX10+
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10-	D86	PEG_TX10-
C32	PCI_AD14	D32	PCI_PAR	C87	GND	D87	GND
C33	PCI_C/BE1#	D33	PCI_SERR#	C88	PEG_RX11+	D88	PEG_TX11+
C34	PCI_PERR#	D34	PCI_STOP#	C89	PEG_RX11-	D89	PEG_TX11-
C35	PCI_LOCK#	D35	PCI_TRDY#	C90	GND (FIXED)	D90	GND (FIXED)
C36	PCI_DEVSEL#	D36	PCI_FRAME#	C91	PEG_RX12+	D91	PEG_TX12+
C37	PCI_IRDY#	D37	PCI_AD16	C92	PEG_RX12-	D92	PEG_TX12-

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Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C38	PCI_C/BE2#	D38	PCI_AD18	C93	GND	D93	GND
C39	PCI_AD17	D39	PCI_AD20	C94	PEG_RX13+	D94	PEG_TX13+
C40	PCI_AD19	D40	PCI_AD22	C95	PEG_RX13-	D95	PEG_TX13-
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	PCI_AD21	D42	PCI_AD24	C97	RSVD	D97	PEG_ENABLE#
C43	PCI_AD23	D43	PCI_AD26	C98	PEG_RX14+	D98	PEG_TX14+
C44	PCI_C/BE3#	D44	PCI_AD28	C99	PEG_RX14-	D99	PEG_TX14-
C45	PCI_AD25	D45	PCI_AD30	C100	GND (FIXED)	D100	GND (FIXED)
C46	PCI_AD27	D46	PCI_IRQC#	C101	PEG_RX15+	D101	PEG_TX15+
C47	PCI_AD29	D47	PCI_IRQD#	C102	PEG_RX15-	D102	PEG_TX15-
C48	PCI_AD31	D48	PCI_CLKRUN#	C103	GND	D103	GND
C49	PCI_IRQA#	D49	PCI_M66EN (*)	C104	VCC_12V	D104	VCC_12V
C50	PCI_IRQB#	D50	PCI_CLK	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

The signals marked with an asterisk symbol (*) are not supported on the conga-BM45.

7.5 Boot Strap Signals

Table 28 Boot Strap Signal Descriptions

Signal	Pin #	Description of Boot Strap Signal	I/O	PU/PD	Comment
AC_SYNC	A29	**Intel® High Definition Audio Sync:** This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		AC_SYNC is a boot strap signal (see caution statement below)
AC_SDOUT	A33	**Intel® High Definition Audio Serial Data Out:** This signal is the serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		AC_SDOUT is a boot strap signal (see caution statement below)
EXCD0_PERST#	A48	ExpressCard Reset	O 3.3V	PU 10k 3.3V	EXCD0_PERST# is a boot strap signal (see caution statement below)
SPKR	B32	Output for audio enunciator, the “speaker” in PC-AT systems	O 3.3V		SPKR is a boot strap signal (see caution statement below)
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	I 1.05V		PEG_LANE_RV# is a boot strap signal (see caution statement below)
SDVO_I2C_DAT (SDVO_DATA) (DDPB_CTRLDATA)	C73	SDVO I²C data line to set up SDVO/HDMI/DisplayPort peripherals.	I/O OD 2.5V		SDVO_I2C_DAT is a boot strap signal (see caution statement below)
PCI_GNT0#	C20	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT0# is a boot strap signal (see caution statement below)
PCI_GNT1#	C18	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT1# is a boot strap signal (see caution statement below)
PCI_GNT2#	C16	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT2# is a boot strap signal (see caution statement below)
PCI_GNT3#	D19	PCI bus master grant output lines, active low.	O 3.3V		PCI_GNT3# is a boot strap signal (see caution statement below)
DDPC_CTRLDATA	D64	Digital Display port C Control Data line to set up HDMI/DisplayPort.	I/O OD 3.3V		DDPC_CTRLDATA is a boot strap signal (see caution statement below)

Caution

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express™ internally implemented resistors or chipset internally implemented resistors that are located on the module. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table with the exception of AC_SYNC, AC_SDOUT, PEG_LANE_RV#, SDVO_I2C_DAT and DDPC_CTRLDATA. External resistors may override the internal strap states and cause the COM Express™ module to malfunction and/or cause irreparable damage to the module.

AC_SYNC and AC_SDOUT can be used to switch PCI Express channels 0-3 between x1 and x4 mode. If both signals are each pulled-up (using 1KΩ resistors) to 3.3V at the rising edge of PWROK then x4 mode is enabled for channels 0-3. x1 mode is used by default if these resistors are not populated. Channel 4 remains configured as x1 mode regardless of the configuration of channels 0-3.

SDVO_I2C_DAT (DDPB_CTRLDATA) can be pulled-up (using 2.2KΩ resistor) to 3.3V in order to set up SDVO/HDMI/DisplayPort peripherals.

PEG_LANE_RV# can be pulled low to activate lane reversal mode.

DDPC_CTRLDATA can be pulled-up (using 2.2KΩ resistor) to 3.3V in order to set up HDMI/DisplayPort.

Note

For more information about implementing a HDMI or DisplayPort interface on COM Express™ carrier boards, refer to application note AN17_HDMI_DP_Implementation.pdf, which can be found on the congatec website.

8 System Resources

8.1 System Memory Map

Table 29 Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(TOM-384kB) – TOM	N.A.	384kB	ACPI reclaim, MPS and NVS area *
(TOM-128MB-384kB) – (TOM-384kB)	N.A.	32MB up to 128MB	VGA frame buffer
1024kB – (TOM-128MB-384kB)	100000 – N.A	N.A.	Extended memory
869kB – 1024kB	E0000 - FFFFF	128kB	Runtime BIOS
832kB – 869kB	D0000 - DFFFF	64kB	Upper memory
640kB – 832kB	A0000 - CFFFF	192kB	Video memory and BIOS
639kB – 640kB	9FC00 - 9FFFF	1kB	Extended BIOS data
0 – 639kB	00000 - 9FC00	512kB	Conventional memory

Note

T.O.M. = Top of memory = max. DRAM installed

** Only if ACPI Aware OS is set to YES in setup.*

8.2 I/O Address Assignment

The I/O address assignment of the conga-BM45 module is functionally identical with a standard PC/AT. The most important addresses and the ones that differ from the standard PC/AT configuration are listed in the table below.

Table 30 I/O Address Assignment

I/O Address (hex)	Size	Available	Description
0000 - 00FF	256 bytes	No	Motherboard resources
0170 - 0177	8 bytes	No	Secondary IDE channel
01F0 - 01F7	8 bytes	No	Primary IDE channels
0376	1 byte	No	Secondary IDE channel command port
0377	1 byte	No	Secondary IDE channel status port
03B0 – 03DF	16 bytes	No	Video system
03F6	1 byte	No	Primary IDE channel command port
03F7	1 byte	No	Primary IDE channel status port
04D0 – 04D1	2 bytes	No	Motherboard resources
0500 – 053F	64 bytes	No	Motherboard resources
0800 – 087F	128 bytes	No	Motherboard resources
0A00 – 0A7F	128 bytes	No	Motherboard resources
0CF8 - 0CFB	4 bytes	No	PCI configuration address register
0CFC - 0CFF	4 bytes	No	PCI configuration data register
0D00 – FFFF		See note	PCI / PCI Express bus

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

8.2.1 LPC Bus

On the conga-BM45 the PCI Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the LPC Bus:

280 – 2FF
3F8 – 3FF
3E8 – 3EF
A00 - A0F

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

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8.3 Interrupt Request (IRQ) Lines

Table 31 IRQ Lines in PIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ or PCI BUS INTx
4	Yes		IRQ4 via SERIRQ or PCI BUS INTx
5	Yes		IRQ5 via SERIRQ or PCI BUS INTx
6	Yes		IRQ6 via SERIRQ or PCI BUS INTx
7	Yes		IRQ7 via SERIRQ or PCI BUS INTx
8	No	Real-time Clock	Not applicable
9	Note 2	SCI / Generic	IRQ9 via SERIRQ or PCI BUS INTx
10	Yes		IRQ10 via SERIRQ or PCI BUS INTx
11	Yes		IRQ11 via SERIRQ or PCI BUS INTx
12	Yes		IRQ12 via SERIRQ or PCI BUS INTx
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	IRQ14 or PCI BUS INTx
15	Note 1	IDE Controller 1 (IDE1) / Generic	IRQ15 or PCI BUS INTx

In PIC mode, the PCI bus interrupt lines can be routed to any free IRQ.

Note

1. *If the SATA configuration in BIOS setup is set to enhanced mode for all SATA ports (serial ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus.*

2. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

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Table 32 IRQ Lines in APIC mode

IRQ#	Available	Typical Interrupt Source	Connected to Pin / Function
0	No	Counter 0	Not applicable
1	No	Keyboard	Not applicable
2	No	Cascade Interrupt from Slave PIC	Not applicable
3	Yes		IRQ3 via SERIRQ
4	Yes		IRQ4 via SERIRQ
5	Yes		IRQ5 via SERIRQ
6	Yes		IRQ6 via SERIRQ
7	Yes		IRQ7 via SERIRQ
8	No	Real-time Clock	Not applicable
9	Note 2	Generic	IRQ9 via SERIRQ, option for SCI
10	Yes		IRQ10 via SERIRQ
11	Yes		IRQ11 via SERIRQ
12	Yes		IRQ12 via SERIRQ
13	No	Math processor	Not applicable
14	Note 1	IDE Controller 0 (IDE0) / Generic	IRQ14
15	Note 1	IDE Controller 1 (IDE1) / Generic	IRQ15
16	No		PIRQA, Integrated VGA Controller, PCI Express Root Port 0, PCI Express Root Port 4, UHCI Host Controller 3
17	No		PIRQB, PCI Express Root Port 1
18	No		PIRQC, EHCI Host Controller 1, PCI Express Root Port 2, UHCI Host Controller 2, SMBus Controller
19	No		PIRQD, PCI Express Root Port 3, UHCI Host Controller 1, Serial ATA Host Controller 1, Serial ATA Host Controller 0 in enhanced/native mode
20	Yes		PIRQE, PCI Bus INTD, onboard Gigabit LAN Controller, option for SCI
21	Yes		PIRQF, PCI Bus INTA
22	Yes		PIRQG, PCI Bus INTB, Intel High Definition Audio Controller
23	Yes		PIRQH, PCI Bus INTC, UHCI Host Controller 0, EHCI Host Controller 0

In APIC mode, the PCI bus interrupt lines are connected with IRQ 20, 21, 22 and 23.

Note

1. *If the SATA configuration is set to enhanced mode in BIOS setup for all SATA ports (serial ATA native mode operation), IRQ14 and 15 are free for PCI/LPC bus.*

2. *In ACPI mode, IRQ9 is used for the SCI (System Control Interrupt). The SCI can be shared with a PCI interrupt line.*

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8.4 PCI Configuration Space Map

Table 33 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	PCI Interrupt Routing	Description
00h	00h	00h	N.A.	Host Bridge
00h	01h	00h	Internal	PCI Express Graphics Root Port
00h	02h	00h	Internal	VGA Graphics
00h	02h	01h	N.A.	VGA Graphics
00h	19h	00h	Internal	Onboard Gigabit LAN Controller
00h	1Ah	00h	Internal	UHCI Host Controller 3
00h	1Ah	07h	Internal	EHCI Host Controller 1
00h	1Bh	00h	Internal	Intel High Definition Audio Controller
00h (see Note)	1Ch	00h	Internal	PCI Express Root Port 0
00h (see Note)	1Ch	01h	Internal	PCI Express Root Port 1
00h (see Note)	1Ch	02h	Internal	PCI Express Root Port 2
00h (see Note)	1Ch	03h	Internal	PCI Express Root Port 3
00h (see Note)	1Ch	04h	Internal	PCI Express Root Port 4
00h	1Dh	00h	Internal	UHCI Host Controller 0
00h	1Dh	01h	Internal	UHCI Host Controller 1
00h	1Dh	02h	Internal	UHCI Host Controller 2
00h	1Dh	07h	Internal	EHCI Host Controller 0
00h	1Eh	00h	Internal	PCI to PCI Bridge
00h	1Fh	00h	N.A.	PCI to LPC Bridge
00h	1Fh	02h	Internal	Serial ATA Controller 0
00h	1Fh	03h	Internal	SMBus Host Controller
00h	1Fh	05h	Internal	Serial ATA Controller 1
01h	04h	xxh	INTA-INTD	PCI Bus Slot 1
01h	05h	xxh	INTA-INTD	PCI Bus Slot 2
01h	06h	xxh	INTA-INTD	PCI Bus Slot 3
01h	07h	xxh	INTA-INTD	PCI Bus Slot 4
02h	00h	xxh	Internal	PCI Express Port 0
03h (see Note)	00h	xxh	Internal	PCI Express Port 1
04h (see Note)	00h	xxh	Internal	PCI Express Port 2
05h (see Note)	00h	xxh	Internal	PCI Express Port 3
06h (see Note)	00h	Xxh	Internal	PCI Express Port 4

Note

The given bus numbers only apply if all PCI Express Ports are enabled in the BIOS setup. If for example PCI Express Port 2 is disabled then PCI Express Port 3 will be assigned bus number 4 instead of bus number 5 and Port 4 will be assigned bus number 5. Furthermore, the respective PCI Express Root Port is hidden if the corresponding PCI Express Port is disabled.

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8.5 PCI Interrupt Routing Map

Table 34 PCI Interrupt Routing Map

PIRQ	PCI BUS INT Line [1]	APIC Mode IRQ	VGA	HDA	UHCI 0	UHCI 1	UHCI 2	UHCI 3	EHCI 0	EHCI 1	SMBus	LAN
A		16	x					x				
B		17										
C		18					x			x	x	
D		19				x						
E	INTD	20										x
F	INTA	21										
G	INTB	22		x								
H	INTC	23			x				x			

Table 35 PCI Interrupt Routing Map (continued)

PIRQ	SATA 0 Native	SATA 1	PCI-EX Root Port 0	PCI-EX Root Port 1	PCI-EX Root Port 2	PCI-EX Root Port 3	PCI-EX Root Port 4	PCI-EX Port 0	PCI-EX Port 1	PCI-EX Port 2	PCI-EX Port 3	PCI-EX Port 4
A			x				x	x [2]	x [5]	x [4]	x [3]	x [2]
B				x				x [3]	x [2]	x [5]	x [4]	x [3]
C					x			x [4]	x [3]	x [2]	x [5]	x [4]
D	x	x				x		x [5]	x [4]	x [3]	x [2]	x [5]
E												
F												
G												
H												

Note

[1] *These interrupts are available for external devices/slots via the C-D connector rows.*

[2] *Interrupt used by single function PCI Express devices (INTA).*

[3] *Interrupt used by multifunction PCI Express devices (INTB).*

[4] *Interrupt used by multifunction PCI Express devices (INTC).*

[5] *Interrupt used by multifunction PCI Express devices (INTD).*

8.6 PCI Bus Masters

The conga-BM45 supports 4 external PCI Bus Masters. There are no limitations in connecting bus master PCI devices.

Note

If there are two devices connected to the same PCI REQ/GNT pair and they are transferring data at the same time then the latency time of these shared PCI devices can not be guaranteed.

8.7 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

8.8 SM Bus

System Management (SM) bus signals are connected to the Intel® I/O Controller Hub 82801GHM (ICH9M-E) and the SM bus is not intended to be used by off-board non-system management devices. For more information about this subject contact congatec technical support.

9 BIOS Setup Description

The following section describes the BIOS setup program. The BIOS setup program can be used to view and change the BIOS settings for the module. Only experienced users should change the default BIOS settings.

9.1 Entering the BIOS Setup Program.

The BIOS setup program can be accessed by pressing the <DEL> key during POST.

9.1.1 Boot Selection Popup

The BIOS offers the possibility to access a Boot Selection Popup menu by pressing the <F11> key during POST. If this option is used a message will be displayed during POST stating that the “Boot Selection Popup menu has been selected” and the menu itself will be displayed immediately after POST thereby allowing the operator to choose the boot device to be used.

9.1.2 Manufacturer Default Settings

Pressing the <End> key repeatedly, immediately after power is initiated will result in the manufacturer default settings being loaded for that boot sequence and only that boot sequence. This is helpful when a previous BIOS setting is no longer desired. If you want to change the BIOS settings, or save the manufacturer default settings, then you must enter the BIOS setup program and use the ‘Save and Exit’ function. This feature is enabled by default and only works with a PS/2 keyboard, it is not available when using a USB keyboard. See setup node in the “BIOS Setup Description” section 9.6.1 “Security Settings”.

9.2 Setup Menu and Navigation

The congatec BIOS setup screen is composed of the menu bar and two main frames. The menu bar is shown below:

Note

Entries in the option column that are displayed in bold print indicate BIOS default values.

Main	Advanced	Boot	Security	Power	Exit

The left frame displays all the options that can be configured in the selected menu. Grayed-out options cannot be configured. Only the blue options can be configured. When an option is selected, it is highlighted in white.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

The setup program uses a key-based navigation system. Most of the keys can be used at any time while in setup. The table below explains the supported keys:

Key	Description
← → Left/Right	Select a setup menu (e.g. Main, Boot, Exit).
↑ ↓ Up/Down	Select a setup item or sub menu.
+ - Plus/Minus	Change the field value of a particular setup item.
Tab	Select setup fields (e.g. in date and time).
F1	Display General Help screen.
F2/F3	Change Colors of setup screen.
F7	Discard Changes.
F9	Load optimal default settings.
F10	Save changes and exit setup.
ESC	Discard changes and exit setup.
ENTER	Display options of a particular setup item or enter submenu.

9.3 Main Setup Screen

When you first enter the BIOS setup, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. The Main screen reports BIOS, processor, memory and board information and is for configuring the system date and time.

Feature	Options	Description
System Time	Hour:Minute:Second	Specifies the current system time. *Note: The time is in 24-hour format.*
System Date	Day of week, month/day/year	Specifies the current system date. *Note: The date is in month-day-year format.*
BIOS ID	no option	Displays the BIOS ID.
Processor	no option	Displays the processor type.
CPU Frequency	no option	Displays CPU frequency.
System Memory	no option	Displays the total amount of system memory.
Product Revision	no option	Displays the hardware revision of the board.
Serial Number	no option	Displays the serial number of the board.
BC Firmware Rev.	no option	Displays the revision of the congatec board controller.
MAC Address	no option	Displays the MAC address of the onboard Ethernet controller.
Boot Counter	no option	Displays the number of boot-ups. (max. 16777215).
Running Time	no option	Displays the time the board is running [in hours max. 65535].

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9.4 Advanced Setup

Select the Advanced tab from the setup menu to enter the Advanced BIOS Setup screen. The menu is used for setting advanced features:

Main	Advanced	Boot	Security	Power	Exit
	ACPI Configuration				
	PCI Configuration				
	Graphics Configuration				
	CPU Configuration				
	Chipset Configuration				
	I/O Interface Configuration				
	Clock Configuration				
	IDE Configuration				
	USB Configuration				
	Keyboard/Mouse Configuration				
	Hardware Health Configuration				
	Watchdog Configuration				

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9.4.1 ACPI Configuration Submenu

Feature	Options	Description
ACPI Aware O/S	No **Yes**	Set this value to allow the system to utilize the Intel ACPI (Advanced Configuration and Power Interface). Set to *NO* for non ACPI aware operating system like DOS and Windows NT. Set to *YES* if your OS complies with the ACPI specification (e.g. Windows 2000, XP)
ACPI Version Features	ACPI v1.0 **ACPI v2.0** ACPI v3.0	ACPI version supported by the BIOS ACPI code and tables.
System Off Mode	**G3/Mech Off** S5/Soft Off	Select the actual power down mode when the system performs a shutdown with a congatec battery system connected. *Note: This node is only visible when the system is connected to a congatec battery system.*
ACPI APIC support	**Enabled** Disabled	Set to enable to include the APIC support table to ACPI.
Suspend mode	**S1 (POS)** S3 (STR)	Select the state used for ACPI system suspend.
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3 resume (required by some OS to re-initialize graphics).
USB Device Wakeup From S3/S4	**Disabled** Enabled	Enable or disable USB device wakeup from S3 and S4 state.
Active Cooling Trip Point	**Disabled** 50, 60, 70, 80, 90°C	Specifies the temperature threshold at which the ACPI aware OS turns the fan on/off.
Passive Cooling Trip Point	Disabled 50, 60, 70, 80, **90**°C	Specifies the temperature threshold at which the ACPI aware OS starts/stops CPU clock throttling.
Critical Trip Point	Disabled, 80, 85, 90, 95, 100, **105**, 110°C	Specifies the temperature threshold at which the ACPI aware OS performs a critical shutdown.
Watchdog ACPI Event	**Shutdown** Restart	Select the event that is initiated by the watchdog ACPI event. When the watchdog times out a critical but orderly OS shutdown or restart can be performed (see note below).

Note

In ACPI mode it is not possible for a "Watchdog ACPI Event" handler to directly restart or shutdown the OS. For this reason the congatec BIOS will do one of the following:

For Shutdown: An over temperature notification is executed. This causes the OS to shut down in an orderly fashion.

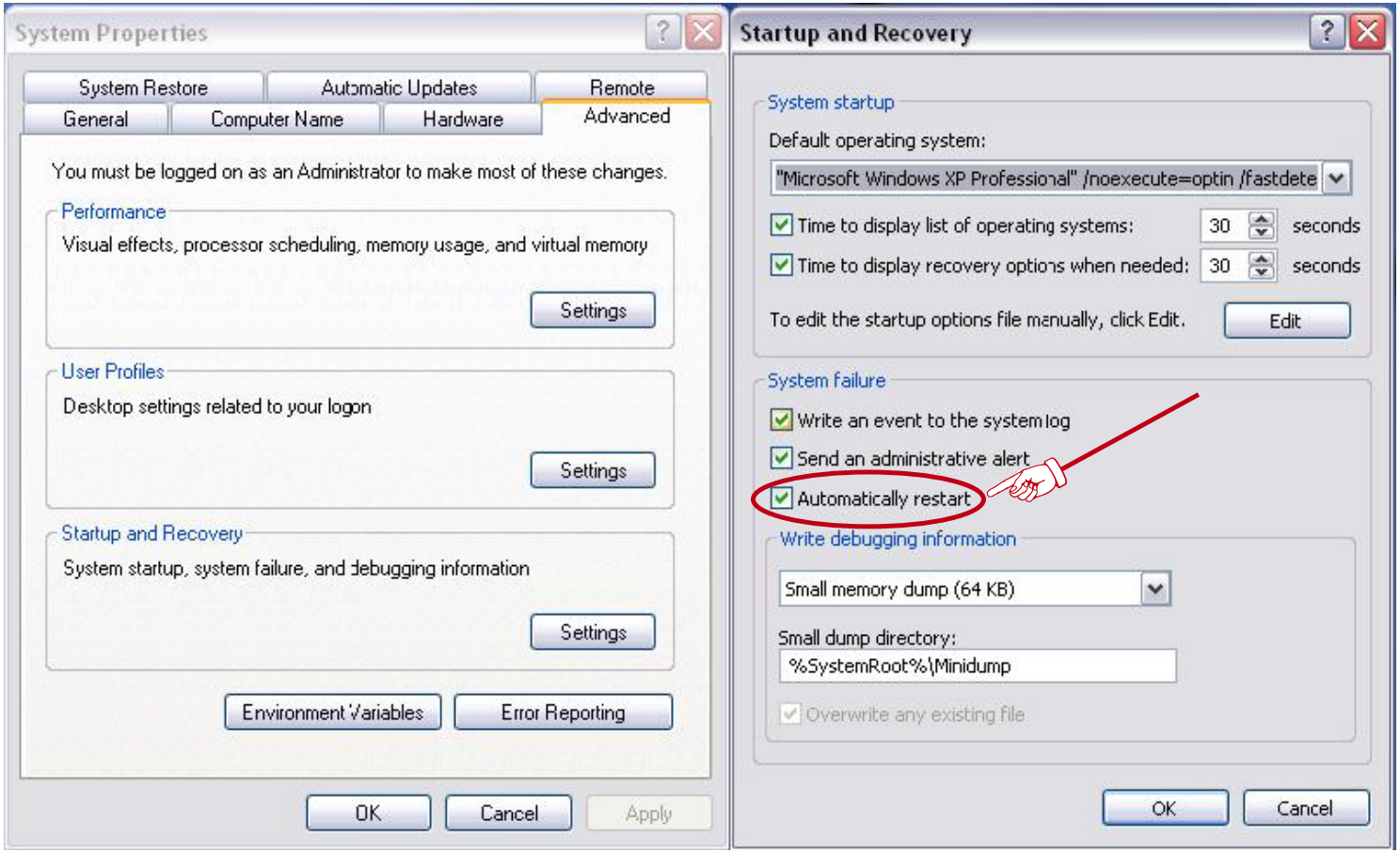
For Restart: An ACPI fatal error is reported to the OS.

It depends on your particular OS as to how this reported fatal error will be handled when the Restart function is selected. If you are using Windows XP/2000 there is a setting that can be enabled to ensure that the OS will perform a restart when a fatal error is detected. After a very brief blue-screen the system will restart.

You can enable this setting buy going to the "System Properties" dialog box and choosing the "Advanced" tab. Once there choose the "Settings"

button for the "Startup and Recovery" section. This will open the "Startup and Recovery" dialog box. In this dialog box under "System failure" there are three check boxes that define what Windows will do when a fatal error has been detected. In order to ensure that the system restarts after a 'Watchdog ACPI Event" that is set to 'Restart', you must make sure that the check box for the selection "Automatically restart" has been checked. If this option is not selected then Windows will remain at a blue-screen after a 'Watchdog ACPI Event" that has been configured for 'Restart' has been generated. Below is a Windows screen-shot showing the proper configuration.

Win XP/2000 Watchdog ACPI Event restart configuration



9.4.2 PCI Configuration Submenu

Feature	Options	Description
Plug & Play O/S	**No** Yes	Specifies if manual configuration is desired. Set to *NO* for operating systems that do not meet the Plug and Play specification. In this case the BIOS configures all devices in the system. Select *YES* to let the operating system configure PnP devices that are not required for booting.
PCI Latency Timer	32, **64**, 96, ... 248	This option allows you to adjust the latency timer of all devices on the PCI bus.
Allocate IRQ to PCI VGA	**Yes** No	Allow or restrict the BIOS from giving the VGA controller an IRQ resource.
Allocate IRQ to SMBUS HC	**Yes** No	Allow or restrict the BIOS from giving the SMBus controller an IRQ resource.
►PCI IRQ Resource Exclusion	sub menu	Opens PCI IRQ Resource Exclusion sub menu.
►PCI Interrupt Routing	sub menu	Opens PCI Interrupt Routing sub menu.

9.4.2.1 PCI IRQ Resource Exclusion Submenu

Feature	Options	Description
IRQ xx	**Available** Reserved	Allow or restrict the BIOS from giving IRQ resource to PCI/PNP devices. *Note: Assigned IRQ resources are shaded and listed as 'Allocated'.*

9.4.2.2 PCI Interrupt Routing Submenu

Feature	Options	Description
PIRQ xx (devices)	**Auto,** 3, 4, .., 14, 15	Select fixed IRQ for PCI interrupt line or set to AUTO to let the BIOS and operating system route an IRQ. *Note: Only those IRQs that are free are listed.*
1st Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.
2nd Exclusive PCI IRQ	**None**, [IRQs assigned manually above]	The selected IRQ will only be assigned to the PIRQ line it has been set to manually. PIRQs set to AUTO will not be assigned this IRQ.

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9.4.3 Graphics Configuration Submenu

Feature	Options	Description
Primary Video Device	IGD PCI/IGD PCI/PEG PEG/IGD **PEG/PCI**	Select primary video adapter to be used during boot up. IGD: Internal Graphics Device PEG: PCI Express x16 Graphics Port Device PCI: Standard PCI Express or PCI Graphics Device
PCIExpress Graphics Port	**Auto**, Enable PEG Always	Choose the configuration of the x16 PEG port. Select Enable PEG Always if Primary Video Device is set to IGD and a x16 PEG card should still be used as secondary graphics card under the target OS.
Internal Graphics Mode Select	Disabled **Enabled, 32MB** Enabled, 64MB Enabled 128MB	This option allows you to disable the internal VGA controller or enable it with up to 256MB initial frame buffer size.
DVMT Memory	128MB **256MB** Maximum DVMT	Amount of DRAM the DVMT graphics driver can allocate.
Boot Display Device	**Auto** CRT only TV only SDVO only CRT + SDVO LFP only CRT + LFP	Select the display device(s) used for boot up. LFP = Local Flat Panel (LVDS) *Note: Auto feature only works with a DDC compatible CRT monitor. SDVO stands for all kinds of true SDVO transmitters as well as for graphic outputs using the SDVO signals like HDMI and Display Port.*
Boot Display Preference	**LFP SDVO-B SDVO-C** LFP SDVO-C SDVO-B SDVO-B SDVO-C LFP SDVO-C SDVO-B LFP	Select order in which devices are checked and enabled as boot display devices in case a combination of LFP and SDVO devices is present. The preference selection is only used if Boot Display Device selection is set to Auto or if SDVO is part of the selection and more than one SDVO device is present.
Always Try Auto Panel Detect	**No** Yes	If set to 'Yes' the BIOS will first look for an EDID data set in an external EEPROM to configure the Local Flat Panel or the SDVO Local Flat Panel. Only if no external EDID data set can be found, the data set selected under 'Local Flat Panel Type' or 'SDVO Local Flat Panel Type' will be used as fallback data set.

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Feature	Options	Description
Local Flat Panel Type	**Auto** VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) SXGA 2x24 (018h) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	Select a predefined LFP type or choose Auto to let the BIOS automatically detect and configure the attached LVDS panel. Auto detection is performed by reading an EDID data set via the video I²C bus. The number in brackets specifies the congatec internal number of the respective panel data set. *Note: Customized EDID™ utilizes an OEM defined EDID™ data set stored in the BIOS flash device.* VGA = 640x480 SVGA = 800x600 XGA = 1024x768 SXGA = 1280x1024 UXGA = 1600x1200
SDVO Local Flat Panel Type	**Disabled** Auto VGA 1x18 (002h) VGA 1x18 (013h) SVGA 1x18 (01Ah) XGA 1x18 (006h) XGA 2x18 (007h) XGA 1x24 (008h) XGA 2x24 (012h) SXGA 2x24 (00Ah) SXGA 2x24 (018h) UXGA 2x24 (00Ch) Customized EDID™ 1 Customized EDID™ 2 Customized EDID™ 3	An SDVO local flat panel is a LVDS panel connected to an SDVO LVDS transmitter on one of the SDVO ports.
Local Flat Panel Scaling	**Centering,** Expand Text, Expand Graphics, Expand Text & Graphics	Select whether and how to scale the actual video mode resolution to the local flat panel resolution.
Backlight Control	**Auto**, 0%, 25%, 50%, 75%, 100%	Select local flat panel backlight control value. If set to Auto, the BIOS tries to read the backlight brightness value from the EPI data set.
Inhibit Backlight	**No** Permanent Until End of POST	Decide whether the backlight on signal should be activated when the panel is activated or whether it should remain inhibited permanently or until the end of BIOS POST.
Invert Backlight Control	**No** Yes	Allow backlight control value inversion if required for the actual backlight hardware controller.
PWM Backlight Control	**Disabled** Enabled	Enable/Disable backlight PWM output of COM Express.

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Feature	Options	Description
SDVO Port B Configuration	Disabled HDMI Port DisplayPort **SDVO DVI** SDVO TV SDVO CRT SDVO LVDS SDVO DVI-Analog	Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port.
SDVO Port C Configuration	Disabled HDMI Port DisplayPort **SDVO DVI** SDVO TV SDVO CRT SDVO LVDS SDVO DVI-Analog	Select the SDVO device connected to this SDVO port or configure the port as HDMI or Display Port.
SDVO/DVI Hotplug Support	**Disabled** Enabled	If set to Enabled the Windows XP/2000 graphics drivers will support 'hotplug' and 'configuration mode persistence' for DVI monitors connected to a DVI SDVO transmitter. Hotplug support means that a DVI monitor connected while the Windows XP/2000 system is already running will automatically be detected and activated. Configuration mode persistence means that, e.g., a dual view DVI configuration will automatically be restored if both DVI monitors are connected again even if during an earlier boot only one DVI monitor had been connected and was active.
Display Mode Persistence	**Disabled** Enabled	Display mode persistence means, that previous display device configurations can be 'remembered' and restored by the system. E.g. a dual view DVI configuration will automatically be restored if both DVI monitors are connected again, even if during an earlier boot only one DVI monitor had been connected and active.
TV Standard	**VBIOS-Default** NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	Select TV standard that should be supported. TV connection type is automatically detected by the Video BIOS.
TV Sub-Type	(Options depend on selected TV standard)	Select sub-type for selected TV standard.

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9.4.4 CPU Configuration Submenu

Feature	Options	Description
Processor Info Block	No option	Displays the processor manufacturer, brand, frequency, and cache sizes.
MPS Revision	1.1 **1.4**	Select the revision of the multi processor support interface that should be offered by the BIOS. Set back to 1.1 in case problems occur with older non ACPI operating systems.
Max CPUID Value Limit	**Disabled** Enabled	When **enabled**, the processor will limit the maximum CPUID input value to **03h** when queried, even if the processor supports a higher CPUID input value. When **disabled**, the processor will return the actual maximum CPUID input value of the processor when queried. Limiting the CPUID input value may be required for older operating systems that cannot handle the extra CPUID information returned when using the full CPUID input value.
Intel® Virtualization Tech.	Disabled **Enabled**	Enable or disable support for Intel® hardware virtualization technology.
Execute-Disable Bit Capability	Disabled **Enabled**	Enable or disable the hardware support for data execution prevention.
Intel® SpeedStep Tech.	Disabled **Enabled**	Disabled: No SpeedStep, default CPU speed. Enabled: CPU speed is controlled by the operating system. *Note: This option is not available for Celeron M CPUs*
Boot CPU Speed On AC	Minimum **Maximum**	Set boot CPU speed when powered by AC. ACPI OS may still change the speed if SpeedStep is enabled.
Boot CPU Speed On Battery	Minimum **Maximum**	Set boot CPU speed when powered by battery. ACPI OS may still change the speed if SpeedStep is enabled.
Intel® C-State Tech.	**Disabled** Enabled	Enable support for standard CPU idle states C2, C3 and C4.
Max. C-State	C1, C2, **C3**, C4, C6	Set the maximum C-state that may be used when C-State Tech. is set to enabled.
Enhanced C-States	**Disabled** Enabled	Enable support for enhanced C-states.

9.4.5 Chipset Configuration Submenu

Feature	Options	Description
Memory Hole	**Disabled** 15MB-16MB	Enable or disable the memory hole between 15MB and 16MB. If enabled, accesses to this range are forwarded to the LPC / PCI bus.
DIMM Thermal Control	**Disabled** 40, 50, 60, 70, 80, 85, 90°C	Select DRAM module environment temperature at which to start memory bandwidth limitation. This should help to control DIMM temperature.
High Precision Event Timer	**Disabled** Enabled	Enable or disable the ICH9M-E high precision event timer (HPET). This timer can be used for precise multimedia or real time application timing. Special software support is required.
HPET Memory Address	**FED00000h** FED01000h FED02000h FED03000h	Set the high precision event timer memory base address.
IOAPIC	Disabled **Enabled**	Enable / Disable ICH9M-E IOAPIC function.
APIC ACPI SCI IRQ	**Disabled** Enabled	If set to Disabled IRQ9 is used for the SCI. If set to Enabled IRQ20 is used for the SCI.
POST Code Output	**PCI** LPC	Select whether port 80h/84h BIOS POST code output should be routed to the PCI bus or the LPC bus.
Active State Power Management	**Disabled** Enabled	Enable or disable PCI Express L0s and L1 link power states.
PCIE Port 0	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 1	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 2	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 3	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE Port 4	**Auto** Enabled Disabled	Enable or disable PCI Express port.
PCIE High Priority Port	**Disabled** Port 0 Port 1 Port 2 Port 3 Port 4	Enable PCI Express high priority port for isochronous data transfers.
Reserve PCIE Hotplug Resources	**No** Yes	Reserve I/O and memory resources for empty PCI Express slots. Setting a PCI Express port to Enabled and reserving resources is required for ExpressCard hotplug support on the respective port.

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Feature	Options	Description
I/O	None **4K** 8K 16K	Number of I/O addresses to reserve for each enabled but empty PCI Express slot.
Memory	None **1MB** 32MB 128MB	Amount of memory to reserve for each enabled but empty PCI Express slot.
Prefetchable Memory	**None** 1MB 32MB 128MB	Amount of prefetchable memory to reserve for each enabled but empty PCI Express slot.
PCIE Port 0 IOxAPIC Enable	**Disabled** Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 1IOxAPIC Enable	**Disabled** Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 2 IOxAPIC Enable	**Disabled** Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 3 IOxAPIC Enable	**Disabled** Enabled	Enable support for IOAPIC behind PCI Express port.
PCIE Port 4 IOxAPIC Enable	**Disabled** Enabled	Enable support for IOAPIC behind PCI Express port.

9.4.6 I/O Interface Configuration Submenu

Feature	Options	Description
HDA Controller	**Enabled** Disabled	Enable onboard Intel® High Definition Audio controller.
Onboard Ethernet Controller	Disabled **Enabled**	Enable or disable the onboard Ethernet controller.
►SIO Winbond W83627 Configuration	sub menu	Opens submenu. *Note: This setup node is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.*
►SIO SMSC SCH3114 Configuration	sub menu	Opens submenu. *Note: This setup node is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.*

9.4.6.1 SIO Winbond W83627 Configuration

Feature	Options	Description
Serial Port 1/2 Configuration	Disabled **3F8/IRQ4** **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Specifies the I/O base address and IRQ of serial port 1/2.
Serial Port 2 Mode	**Normal** IrDA ASK IR	Specifies the mode for serial port 2.
IR Duplex Mode	Full Duplex **Half Duplex**	Select IRDA full or half duplex function.
IR I/O Pin Select	SINB/SOUTB **IRRX/RTX**	Select receiver and transmit pins for IRDA mode.
Parallel Port Address	**Disabled** 378 278 3BC	Specifies the I/O base address used by the parallel port.
Parallel Port Mode	**Normal** Bi-directional ECP EPP ECP&EPP	Specifies the parallel port mode.
EPP Version	**1.9** 1.7	Specifies the EPP version.
Parallel Port DMA	DMA0 DMA1 **DMA3**	Specifies the DMA channel for parallel port in ECP mode.
Parallel Port IRQ	None IRQ5 **IRQ7**	Specifies the interrupt for the parallel port.

Note

This setup menu is only available if an external Winbond W83627 Super I/O has been implemented on the carrier board.

9.4.6.2 SIO SMSC SCH3114 Configuration

Feature	Options	Description
Serial Port 1/2/3/4 Address	**Disabled** 3F8 2F8 3E8 2E8	Specifies the I/O base address of serial port 1/2/3/4.
Serial Port 1/2/3/4 IRQ	3 4 10 11	Specifies the interrupt of serial port 1/2/3/4.
Serial Port 2 Mode	**Normal** IrDA ASK IR	Select serial port 2 mode.
IR Duplex Mode	**Full Duplex** Half Duplex	Serial port 2 infrared duplex mode.
Receiver Polarity	**High** Low	Serial port 2 infrared receiver polarity.
Xmitter Polarity	High **Low**	Serial port 2 infrared transmitter polarity.

Note

This setup menu is only available if an external SMSC SCH3114 Super I/O has been implemented on the carrier board.

9.4.7 Clock Configuration

Feature	Options	Description
Spread Spectrum	**Disabled** Enabled	Enable spread spectrum clock modulation to reduce EMI.

9.4.8 IDE Configuration Submenu

Feature	Options	Description
SATA Port 0/1	Disabled **Compatible** Enhanced	Configure the IDE controller handling SATA ports 0 and 1. Disabled: The controller and both ports are disabled. Compatible: The controller operates in legacy or compatible mode. Enhanced: The controller operates in enhanced or native mode.
Configure SATA Port 0/1 as	**IDE** RAID AHCI	Further configure the IDE controller handling SATA ports 0 and 1 *Note: This node only becomes available if SATA Port 0/1 is set to Enhanced.*
SATA Port 0/1 Hotplug	**Disabled** Enabled	Enable or disable SATA device hotplug support. This node and the hotplug feature only become available if *SATA Port 0/1* is set to *Enhanced* and *Configure SATA Port 0/1 as* is set to *RAID* or *AHCI*.
SATA Port 2/3 (optional PATA Port)	Disabled **Enabled**	Enable or disable the IDE controller handling SATA ports 2 and 3 *Note: A SATA to PATA converter is optionally connected to SATA port 3. This SATA to PATA converter offers support for one parallel ATA device.*
PATA Detection Time Out (s)	0, 1, 2, 3, 5, 10, 15, 30	Select how long the BIOS should try to detect a PATA drive behind the SATA to PATA converter connected to SATA port 3 (optional).
►Primary IDE Master	sub menu	Reports type of connected IDE device.
►Secondary IDE Master	sub menu	Reports type of connected IDE device.
►Third IDE Master	sub menu	Reports type of connected IDE device.
►Fourth IDE Master	sub menu	Reports type of connected IDE device.
Hard Disk Write Protect	**Disabled** Enabled	If enabled, protects the hard drive from being erased. Disabled allows the hard drive to be used normally. Read, write and erase functions can be performed to the disk.
IDE Detect Time Out (s)	0, 5, 10, ... 30, **35**	Set this option to stop the BIOS from searching for IDE devices within the specified number of seconds. Basically, this allows you to fine-tune the settings to allow for faster boot times. Adjust this setting until a suitable timing can be found that will allow for all IDE disk drives that are attached to be detected.

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9.4.8.1 Primary/Secondary IDE Master/Slave Submenu

Feature	Options	Description
Device	Hard Disk ATAPI CDROM	Displays the type of drive detected. The 'grayed-out' items below are the IDE disk drive parameters taken from the firmware of the IDE disk
Vendor	no option	Manufacturer of the device.
Size	no option	Total size of the device.
LBA Mode	supported not supported	Shows whether the device supports Logical Block Addressing.
Block Mode	number of sectors	Block mode boosts IDE performance by increasing the amount of data transferred. Only 512 byte of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 kB per interrupt.
PIO Mode	0, 1, 2, 3, 4	IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. If PIO mode increases, the cycle time decreases.
Async DMA	no option	This indicates the highest Asynchronous DMA Mode that is supported.
Ultra DMA	no option	This indicates the highest Synchronous DMA Mode that is supported.
S.M.A.R.T	no option	Self-Monitoring Analysis and Reporting Technology protocol used by IDE drives of some manufacturers to predict drive failures.
Type	Not Installed **Auto** CD/DVD ARMD	Sets the type of device that the BIOS attempts to boot from after the POST has completed. *Not Installed* prevents the BIOS from searching for an IDE disk. *Auto* allows the BIOS to auto detect the IDE disk drive type. *CD/DVD* specifies that an IDE CD/DVD drive is attached. The BIOS will not attempt to search for other types of IDE disk drives. *ARMD* specifies an ATAPI Removable Media Device. This includes, but is not limited to ZIP and LS-120.
LBA/Large Mode	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect LBA mode control. Set to Disabled to prevent the BIOS from using LBA mode.
Block (Multi-Sector Transfer)	Disabled **Auto**	Set to *AUTO* to let the BIOS auto detect device support for multi sector transfer. The data transfer to and from the device will occur multiple (the number of sectors, see above) sectors at a time. Set to Disabled to prevent the BIOS from using block mode. The data transfer to and from the device will occur one sector at a time.
PIO Mode	**Auto** 0, 1, 2, 3, 4	Set to *AUTO* to let the BIOS auto detect the supported PIO mode.
DMA Mode	**Auto** Disabled SWDMA 1, 2 MWDMA0, 1, 2 UDMA0, 1, 2, 3, 4, 5, 6	Set to *AUTO* to let the BIOS auto detect the supported DMA mode. SWDMA = Single Word DMA MWDMA = Multi Word DMA UDMA = Ultra DMA
S.M.A.R.T	**Auto** Disabled Enabled	Set to *AUTO* to let the BIOS auto detect hard disk drive support. Set to *Disabled* to prevent the BIOS from using SMART feature. Set to *Enabled* to allow the BIOS to use SMART feature on supported hard disk drives.
32Bit Data Transfer	Disabled **Enabled**	Enable/Disable 32-bit data transfers on supported hard disk drives.
ARMD Emulation Type	**Auto** Floppy Hard disk drive	ARMD is a device that uses removable media, such as the LS120, MO (Magneto-optical), or Iomega Zip drives. If you want to boot from media on ARMD, it is required that you emulate boot up from a floppy or hard disk drive. This is essentially necessary when trying to boot to DOS. You can select the type of emulation used if you are booting such a device.

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9.4.9 USB Configuration Submenu

Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports **8 USB Ports**	Disable ICH9M-E USB host controllers. Enable UHCI host controller 0. Enable UHCI host controller 0 + 1. Enable UHCI host controller 0 + 1 + 2. Enable UHCI host controller 0 + 1 + 2 + 3.
USB 2.0 Controller	**Enabled** Disabled	Enable the ICH9M-E USB 2.0 (EHCI) host controller.
Legacy USB Support	Disabled **Enabled** Auto	Legacy USB Support refers to the USB keyboard, USB mouse and USB mass storage device support. If this option is *Disabled*, any attached USB device will not become available until a USB compatible operating system is booted. However, legacy support for USB keyboard will be present during POST. When this option is *Enabled*, those USB devices can control the system even when there is no USB driver loaded. *AUTO* disables legacy support if no USB devices are connected.
USB Legacy POST-Always	**Enabled** Disabled	If set to Enabled, USB legacy support is always available at least during BIOS POST regardless of the main legacy USB support setting. This ensures that the BIOS setup can always be entered and modified using a USB keyboard. Setting this node and the main node Legacy USB Support both to Disabled completely disables BIOS legacy USB support. This decreases BIOS boot time but also disables BIOS setup access using a USB keyboard.
USB Keyboard Legacy Support	Disabled **Enabled**	Enable/Disable USB keyboard legacy support. *NOTE: This option has to be used with caution. If the system is equipped with USB keyboard only then the user cannot enter setup to enable the option back*
USB Mouse Legacy Support	Disabled **Enabled**	Enable/Disable USB mouse legacy support.
USB Storage Device Support	Disabled **Enabled**	Enable/Disable USB mass storage device support.
Port 64/60 Emulation	Disabled **Enabled**	Enable/Disable the “Port 6h/64h” trapping option. Port 60h/64h trapping allows the BIOS to provide full PS/2 based legacy support for USB keyboard and mouse. It provides the PS/2 functionality such as keyboard lock, password setting, scan code selection etc. to USB keyboards.
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 host controller in HiSpeed (480Mbps) or Full Speed (12Mbps).
BIOS EHCI Hand-Off	**Disabled** Enabled	Enable workaround for OSes without EHCI hand-off support.
USB Beep Message	Disabled **Enabled**	Enable/Disable the beep during USB device enumeration.
USB Stick Default Emulation	Auto **Hard Disk**	Select default USB stick emulation type. Auto selects floppy or hard disk emulation based on the storage size of the USB stick, but the emulation type can be manually reconfigured for each device using the Mass Storage Device Configuration sub menu.
USB Mass Storage Reset Delay	10 Sec 20 Sec 30 Sec 40 Sec	Number of seconds the legacy USB support BIOS routine waits for the USB mass storage device after the start unit command.
►USB Mass Storage Device Configuration	sub menu	Opens sub menu.

9.4.9.1 USB Mass Storage Device Configuration Submenu

Feature	Options	Description
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	Every USB MSD that is enumerated by the BIOS will have an emulation type setup option. This option specifies the type of emulation the BIOS has to provide for the device. *Note: The device's formatted type and the emulation type provided by the BIOS must match for the device to boot properly.* Select *AUTO* to let the BIOS auto detect the current formatted media. If Floppy is selected then the device will be emulated as a floppy drive. *Forced FDD* allows a hard disk image to be connected as a floppy image. Works only for drives formatted with FAT12, FAT16 or FAT32. *Hard Disk* allows the device to be emulated as hard disk. *CDROM* assumes the CD.ROM is formatted as bootable media, specified by the 'El Torito' Format Specification.

9.4.10 Keyboard/Mouse Configuration Submenu

Feature	Options	Description
Bootup Num-Lock	Off **On**	Specifies the power-on state of the Num-lock feature on the numeric keypad of the keyboard.
Typematic Rate	Slow **Fast**	Specifies the rate at which the computer repeats a key that is held down. *Slow* sets a rate of under 8 times per second. *Fast* sets a rate of over 20 times per second.
PS/2 Mouse Support	**Disabled** Enabled Auto	Configure PS/2 mouse support. *Note: PS/2 support for mouse or keyboard is only available if a Winbond W83627 Super I/O or a SMSC SCH3114 Super I/O has been implemented on the carrier board.*

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9.4.11 Hardware Monitoring Submenu

Feature	Options	Description
H/W Health Function	Disabled **Enabled**	Enable hardware health monitoring device and display the readings.
Board Temperature	no option	Current board temperature.
CPU Temperature	no option	Current processor die temperature.
Top DIMM Environment Temperature	no option	Environment temperature of the top side DIMM.
Bottom DIMM Environment Temperature	no option	Environment temperature of the bottom side DIMM.
CPU Fan Speed	no option	Current CPU FAN speed.
VcoreA	no option	Current Core A reading.
+3.3VSB	no option	Current 3.3V standby reading.
+5VSB	no option	Current 5V standby reading.
+12Vin	no option	Current 12 V in reading.
VRTC	no option	Current VRTC reading.

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9.4.12 Watchdog Configuration Submenu

Feature	Options	Description
POST Watchdog	**Disabled** 30sec 1min 2min 5min 10min 30min	Select the timeout value for the POST watchdog. The watchdog is only active during the power-on-self-test of the system and provides a facility to prevent errors during boot up by performing a reset..
Stop the Watchdog for User Interaction	No **Yes**	Select whether the POST watchdog should be stopped during the popup boot selection menu or while waiting for setup password insertion.
Runtime Watchdog	**Disabled** One time trigger Single Event Repeated Event	Selects the operating mode of the runtime watchdog. This watchdog will be initialized just before the operating system starts booting. If set to '*One time trigger'* the watchdog will be disabled after the first trigger. If set to *'Single event'*, every stage will be executed only once, then the watchdog will be disabled. If set to *'Repeated event'* the last stage will be executed repeatedly until a reset occurs.
Delay	see Post Watchdog	Select the delay time before the runtime watchdog becomes active. This ensures that an operating system has enough time to load.
Event 1	**NMI** ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 1 is reached. For more information about *ACPI Event* see section 9.4.1 of this user's guide.
Event 2	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 2 is reached.
Event 3	**Disabled** NMI ACPI Event Reset Power Button	Selects the type of event that will be generated when timeout 3 is reached.
Timeout 1	0.5sec 1sec 2sec 5sec **10sec** 30sec 1min 2min	Selects the timeout value for the first stage watchdog event.
Timeout 2	see above	Selects the timeout value for the second stage watchdog event.
Timeout 3	see above	Selects the timeout value for the third stage watchdog event.

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9.5 Boot Setup

Select the Boot tab from the setup menu to enter the Boot setup screen. In the upper part of the screen the Boot setup allows you to prioritize the available boot devices. The lower part of this setup screen shows options related to the BIOS boot.

9.5.1 Boot Device Priority

Feature	Options	Description
Boot Priority Selection	Device Based **Type Based**	Select between device and type based boot priority lists. The “Device Based” boot priority list allows you to select from a list of currently detected devices only. The “Type Based” boot priority list allows you to select device types, even if a respective device is not yet present. Moreover, the “Device Based” boot priority list might change dynamically in cases when devices are physically removed or added to the system. The “Type Based” boot menu is static and can only be changed by the user.
1st, 2nd, 3rd, ... Boot Device (Up to 12 boot devices can be prioritized if device based priority list control is selected. If “Type Based” priority list control is enabled only 8 boot devices can be prioritized.)	Disabled Primary Master Primary Slave Secondary Master Secondary Slave Legacy Floppy USB Hard disk USB CDROM USB Removable Dev. Onboard LAN External LAN PCI Mass Storage PCI SCSI Card Any PCI BEV Device Third Master Third Slave PCI RAID Local BEV ROM Fourth Master Fourth Slave	This view is only available when in the default “Type Based” mode. When in “Device Based” mode you will only see the devices that are currently connected to the system. The default boot priority is *Removables 1st, ATAPI CDROM 2nd, Hard Disk 3rd, BEV 4th* (BEV = Boot Entry Vector, e.g. Network or SCSI Option-ROMs).

9.5.2 Boot Settings Configuration

Feature	Options	Description
Quick Boot	Disabled **Enabled**	If *Enabled*, some POST tasks will be skipped to speed-up the BIOS boot process.
Quiet Boot	**Disabled** Enabled	*Disabled* displays normal POST diagnostic messages. *Enabled* displays OEM logo instead of POST messages. *Note: The default OEM logo is a dark screen.*
Boot Display	**Clear** Maintain	Controls the end of POST boot display handling, if Quiet Boot is enabled. If set to *Maintain* the BIOS will maintain the current display contents and graphics video mode used for POST display. If set to *Clear* the BIOS will clear the screen and switch to VGA text mode at end of POST.
Automatic Boot List Retry	**Disabled** Enabled	
Add-On ROM Display Mode	**Force BIOS** Keep current	Set display mode for Option ROM.
Halt On Error	**Disabled** Enabled	Determines whether the BIOS halts and displays an error message if an error occurs. If set to *Enabled* the BIOS waits for user input.
Hit 'DEL' Message Display	Disabled **Enabled**	Allows/Prevents the BIOS to display the '*Hit Del to enter Setup'* message.
Interrupt 19 Capture	**Disabled** Enabled	Allows/Prevents the option ROMs (such as network controllers) from trapping the boot strap interrupt 19.
PXE Boot to LAN	**Disabled** Enabled	Disable/Enable PXE boot to LAN *Note: When set to 'Enabled', the system has to be rebooted in order for the Intel Boot Agent device to be available in the Boot Device Menu.*
Power Loss Control (see note below)	**Remain Off** Turn On Last State	Specifies the mode of operation if an AC power loss occurs. *Remain Off* keeps the power off until the power button is pressed. *Turn On* restores power to the computer. *Last State* restores the previous power state before power loss occurred. *Note: Only works with an ATX type power supply.*

Note

1. *The term 'AC power loss' stands for the state when the module looses the standby voltage on the 5V_SB pins. On congatec modules, the standby voltage is continuously monitored after the system is turned off. If within 30 seconds the standby voltage is no longer detected, then this is considered an AC power loss condition. If the standby voltage remains stable for 30 seconds, then it is assumed that the system was switched off properly.*

2. *Inexpensive ATX power supplies often have problems with short AC power sags. When using these ATX power supplies it is possible that the system turns off but does not switch back on, even when the PS_ON# signal is asserted correctly by the module. In this case, the internal circuitry of the ATX power supply has become confused. Usually another AC power off/on cycle is necessary to recover from this situation.*

3. *Unlike other module designs available in the embedded market, a CMOS battery is not required by congatec modules to support the 'Power Loss Control' feature.*

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9.6 Security Setup

Select the Security tab from the setup menu to enter the Security setup screen.

9.6.1 Security Settings

Feature	Options	Description
Supervisor Password	Installed Not Installed	Reports if there is a supervisor password set.
User Password	Installed Not Installed	Reports if there is a user password set.
Change Supervisor Password	enter password	Specifies the supervisor password.
User Access Level	No Access View Only Limited **Full Access**	Sets BIOS setup utility access rights for user level.
Boot Selection Popup Menu Access	**Anybody** Setup User Setup Supervisor No Access	Select who can access the boot selection popup menu when setup passwords are installed.
Change User Password	enter password	Specifies the user password.
Password Check	**Setup** Always	Setup: Check password while invoking setup Always: Check password also on each boot.
Boot Sector Virus Protection	**Disabled** Enabled	Select *Enabled* to enable boot sector protection. The BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. If enabled, the following appears when a write is attempted to the boot sector. You may have to type N several times to prevent the boot sector write. *Boot Sector Write!* *Possible VIRUS: Continue (Y/N)?* The following appears after any attempt to format any cylinder, head or sector of any hard disk drive via the BIOS INT13 hard disk drive service: *Format!!!* *Possible VIRUS: Continue (Y/N)?*
HDD Security Freeze Lock	Disabled **Enabled**	If enabled, the BIOS will send the Security Freeze Lock command to each attached hard disk supporting the security command set. This will prevent anybody from setting or changing a hard disk password after POST.
Ask HDD Password on Every Boot	**No** Yes	Select whether the hard disk unlock password must be entered on each boot. Only applicable if a hard disk user password is installed (see section 9.6.2 Hard Disk Security).
BIOS Update & Write Protection	**Disabled** Enabled	Only visible if a supervisor password is installed. If enabled the BIOS update and modification utilities will ask for the supervisor password before allowing any write accesses to the BIOS flash ROM chip.
END-Key Loads CMOS Defaults	**Yes** No	If set to Yes, the user can force the loading of CMOS defaults by pressing the END key during POST.

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9.6.2 Hard Disk Security

This feature enables the users to set, reset or disable passwords for each hard drive in Setup without rebooting. If the user enables password support, a power cycle must occur for the hard drive to lock using the new password. Both user and master password can be set independently however the drive will only lock if a user password is installed.

9.6.2.1 Hard Disk Security User Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD User Password	enter password	Set or clear the user password for the hard disk. *Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.*

9.6.2.2 Hard Disk Security Master Password

Feature	Options	Description
Primary/Secondary Master/Slave HDD Master Password	enter password	Set or clear the master password for the hard disk. *Note: This option will be shaded if the hard drive does support the Security Mode Feature set but user failed to unlock the drive during BIOS POST.*

9.7 Power Setup

Select the Power tab from the setup menu to enter the Power Management setup screen.

Feature	Options	Description
Power Management / APM	Disabled **Enabled**	Set this option to allow or prevent chipset power management and APM (Advanced Power Management).
Suspend Timeout	**Disabled** 1- 60 Min	Specifies the length of time of inactivity the system waits before it enters suspend mode.
Video Power Down Mode	Disabled Standby **Suspend**	Specifies the power state that the video subsystem enters when the BIOS places it in a power saving state after the specified period of display inactivity has expired.
Hard Disk Power Down Mode	Disabled Standby **Suspend**	Specifies the power state that the hard disk drives enter after the specified period of hard drive inactivity has expired.
<Device>	Ignore **Monitor**	Determines whether the device activity is monitored by the power management timer or not.
Resume On Ring	**Disabled** Enabled	Disable / enable RI signal (= GPE2 on pin 89 of X4 connector) to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On PME	**Disabled** Enabled	Disable / enable PCI PME to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
Resume On RTC Alarm	**Disabled** Enabled	Disable / enable RTC to generate a wake event. If enabled wake is possible from all power down states including S5 (Soft Off).
RTC Alarm Date (Days)	**Everyday**, 01....31	Select the day of the month when the event should be generated.
System Time	Hour:Minute:Second	Select the system time when the event should be generated.
Power Button Mode	**On/Off** Suspend	Specifies if the system enters suspend or soft off mode when the power button is pressed.

9.7.1 Exit Menu

Select the Exit tab from the setup menu to enter the Exit setup screen.

You can display an Exit screen option by highlighting it using the <Arrow> keys.

Feature	Description
Save Changes and Exit	Exit setup and reboot so the new system configuration parameters can take effect.
Discard Changes and Exit	Exit setup without saving any changes made in the BIOS setup program.
Discard Changes	Discard changes without exiting setup. The option values presented when the computer was turned on are used.
Load CMOS Defaults	Load the CMOS defaults of all the setup options.

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10 Additional BIOS Features

The conga-BM45 uses a congatec/AMIBIOS that is stored in an onboard Flash Rom chip and can be updated using the congatec System Utility, which is available in a DOS based command line, Win32 command line, Win32 GUI, and Linux version.

The BIOS displays a message during POST and on the main setup screen identifying the BIOS project name and a revision code. The initial production BIOS is identified as BM45R1xx, where BM45 is the congatec internal project name, R is the identifier for a BIOS ROM file, 1 is the so called feature number and xx is the major and minor revision number.

10.1 Updating the BIOS

BIOS updates are often used by OEMs to correct platform issues discovered after the board has been shipped or when new features are added to the BIOS.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility, which is called CGUTLm1x.pdf and can be found on the congatec AG website at www.congatec.com.

10.2 BIOS Recovery

The “BIOS recovery” scenario is recommended for situations when the normal flash update fails and the user can no longer boot back to an OS to restore the system. The code that handles BIOS recovery resides in a section of the flash referred to as “boot block”.

For more information about “BIOS Recovery” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.

10.2.1 BIOS Recovery via Storage Devices

In order to make a BIOS recovery from a floppy disk, CD-ROM (ISO9660) or USB floppy the BIOS file must be copied into the root directory of the storage device and renamed AMIBOOT.ROM.

For more information about “BIOS Recovery via Storage Devices” refer to application note AN6_BIOS_Recovery.pdf, which can be found on the congatec AG website at www.congatec.com.t

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10.3 BIOS Security Features

The BIOS provides both a supervisor and user password. If you use both passwords, the supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when setup is executed.

The two passwords activate two different levels of security. If you select password support you are prompted for a one to six character password. Type the password on the keyboard. The password does not appear on the screen when typed.

The supervisor password (supervisor mode) gives unrestricted access to view and change all the setup options. The user password (user mode) gives restricted access to view and change setup options.

If only the supervisor password is set, pressing <Enter> at the password prompt of the BIOS setup program allows the user restricted access to setup.

Setting the password check to 'Always' restricts who can boot the system. The password prompt will be displayed before the system attempts to load the operating system. If only the supervisor password is set, pressing <Enter> at the prompt allows the user to boot the system.

10.4 Hard Disk Security Features

Hard Disk Security uses the Security Mode feature commands defined in the ATA specification. This functionality allows users to protect data using drive-level passwords. The passwords are kept within the drive, so data is protected even if the drive is moved to another computer system.

The BIOS provides the ability to 'lock' and 'unlock' drives using the security password. A 'locked' drive will be detected by the system, but no data can be accessed. Accessing data on a 'locked' drive requires the proper password to 'unlock' the disk.

The BIOS enables users to enable/disable hard disk security for each hard drive in setup. A master password is available if the user can not remember the user password. Both passwords can be set independently however the drive will only lock if a user password is installed. The max length of the passwords is 32 bytes.

During POST each hard drive is checked for security mode feature support. In case the drive supports the feature and it is locked, the BIOS prompts the user for the user password. If the user does not enter the correct user password within five attempts, the user is notified that the drive is locked and POST continues as normal. If the user enters the correct password, the drive is unlocked until the next reboot.

In order to ensure that the ATA security features are not compromised by viruses or malicious programs when the drive is typically unlocked, the BIOS disables the ATA security features at the end of POST to prevent their misuse. Without this protection it would be possible for viruses or malicious programs to set a password on a drive thereby blocking the user from accessing the data.

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11 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

Specification	Link
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
PCI Specification, Revision 2.2	http://www.pcisig.com/specifications
Serial ATA Specification, Revision 1.0a	http://www.serialata.org
PICMG® COM Express Module™ Base Specification	http://www.picmg.org/
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications

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